DATUM TII

TIMING DIVISION

INSTRUCTION MANUAL
MODEL 9400
DIGITAL READER
PART NUMBER 9400-610

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SECTION I
SYSTEM DESCRIPTION

1.1 GENERAL

The DATUM Model 9400-610 DIGITAL READER accepts a serial digital code as its input, decodes this code and extracts binary time-of-day and other digital data. The recovered digital data is provided to the user in a parallel form. The recovered binary time data is converted into a binary coded decimal (BCD) format. This BCD time data is 1) used to drive a time-of-day display located on the front panel and 2) multiplexed into a four-line format to drive a DATUM Model 9300-713 Time Code Generator/Reader.

Front panel controls are provided to allow for selection of one of seven tape deck speeds, one of four input code sources, local or remote control operation and operating mode.

Front panel alarm indicators are provided to indicate loss of input code, time or parity errors and to indicate a defective primary power fuse.

Refer to the Top Assembly Drawing in Section IX for physical location of controls and indicators.

1.2 PHYSICAL

The DATUM Model 9400-610 is constructed in a 1 3/4-inch package requiring minimum 19-inch rack mounting. The unit offers easy handling for desk-top mounting. A decimal time-of-day display on the front panel indicates time-of-day as recovered from the input code.

SECTION II

SPECIFICATIONS

2.1 INPUTS

2.1.1 AC POWER

A.	Voltage:	115/230 volts AC
B.	Frequency:	50-400 Hz
C.	Power:	Less than 1 ampere

2.1.2 INPUT CODE

A.	Format:	Digital code per Fig. 2-1
B.	Levels:	Binary 1: +3.7V±1.3V Binary 0: +0.2V±0.2V
C.	Input Impedance:	DTL/TTL compatible

2.1.3 I/O CONTROL

A. 7 lines of remote control inputs

B.	Levels:	Binary 1: +3.7V±1.3V Binary 0: +0.2V±0.2V
C.	Input Impedance:	DTL/TTL compatible

D. Refer to Section VII for pin assignments

2.2 OUTPUTS

2.2.1 DATA OUTPUT

A. 37 bits, representing 32 data bits (2-33), loss of input, time and parity error alarms plus data ready and output strobe pulses.

B.	Output Levels:	Binary 1: +3.7V±1.3V Binary 0: +0.2V±0.2V
C.	Output Impedance:	DTL/TTL compatible

D. Refer to Section VII for pin assignments.

2.2.2 I/O CONTROL

A. 12 bits, representing four bits of multiplexed time-of-day, six strobe pulses, tape search enable pulse and frame rate pulse.

B.	Levels:	Binary 1: +3.7V±1.3V Binary 0: +0.2V±0.2V
C.	Output Impedance:	DTL/TTL compatible

D. Refer to Section VII for pin assignments.

2.3 TIME BASE

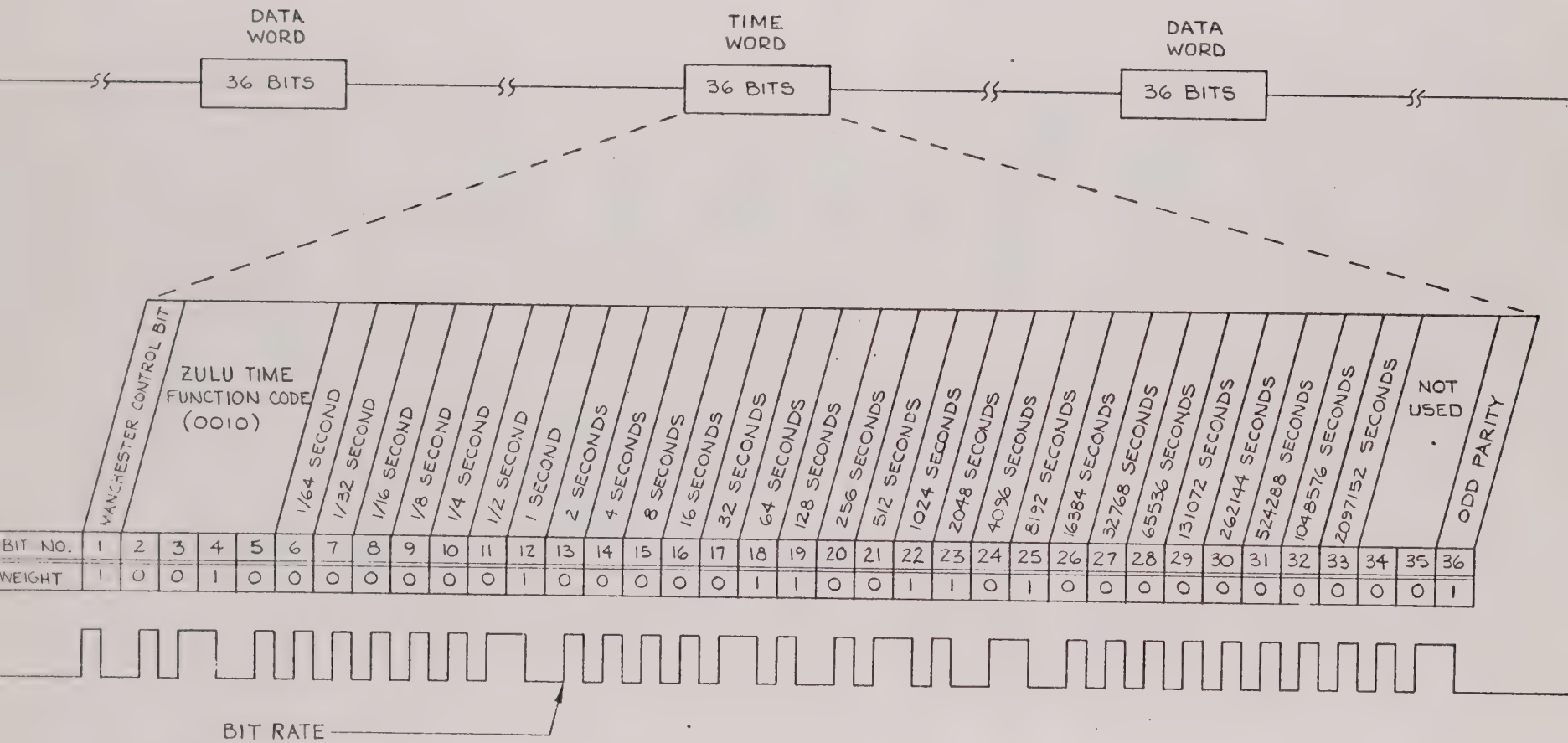
A.	Type:	Crystal Controlled Oscillator
B.	Frequency:	1 MHz
C.	Stability:	$\pm 5 \times 10^{-6}$

2.4 ENVIRONMENT

A.	Temperature:	0° to +50°C
B.	Humidity:	Up to 95% relative

2.5 PHYSICAL

A.	Panel Height:	1-3/4 inches
B.	Chassis Width:	17 inches (19 inches with mounting brackets)
C.	Chassis Depth:	18 inches



AT:

3 3/4 IPS	3KHz
7 1/2 IPS	6KHz
15 IPS	12KHz
30 IPS	24KHz
60 IPS	48KHz
120 IPS	96KHz
300 IPS	240KHz

TIME DEPICTED IS 11,457 SECONDS/3 HOURS, 10 MINUTES, 57 SECONDS

Figure 2-1.

SECTION III

OPERATING PROCEDURES

3.1 OPERATING CONTROLS AND INDICATORS

A. SPEED SELECT: Used to select the operating speed of the Digital Reader during local operation.

B. CODE SOURCE

1) DECK 1, 2: Used to select either of two tape decks

2) INPUT 1,2: Used to select either of two tracks from the selected tape deck.

C. CONTROL

1) LOCAL/REMOTE: Used to select either the front panel (LOCAL) or external (REMOTE) control of operating mode.

2) FWD/REV: Used to condition the unit for forward or reverse tape motion during local operation.

D. POL NORM/INV: Used to condition the unit to accept either normal or inverted polarity input code during local operation.

E. INPUT LOSS: Indicates loss of digital code input.

F. TIME ERROR: Indicates a time discrepancy between the contents of the shift register and the contents of the Major Time Counter.

G. PARITY ERROR: Indicates a parity discrepancy between the parity of the first 35 shift register outputs and the decoded parity bit (Bit 36).

H. FUSE BLOWN: Indicates an open primary power fuse.

3.2 OPERATING PROCEDURES

3.2.1 Connect input and output connectors as required. Refer to Section II for specifications.

3.2.2 Apply AC power to the unit by placing the POWER switch in the ON position.

3.2.3 LOCAL Control

A. Place the LOCAL/REMOTE switch in the LOCAL position.

B. Use the SPEED SELECT switch to select the desired playback rate.

NOTE: SEARCH corresponds to a tape speed of 300 inches per second

3.2.3 Continued

C. Use the CODE SOURCE controls to select the desired tape transport and track for the input code.

D. Set the FWD/REV switch to correspond to the tape operating direction.

E. Set the POL switch to correspond to the polarity of the input code.

3.2.4 REMOTE CONTROL

A. Place the LOCAL/REMOTE switch in the REMOTE position.

B. Select operating speed by controlling the four speed control lines (Drawing No. 17685, sheet 15) according to the following table:

IPS	SPC1	SPC2	SPC4	$\overline{ESS}$
3-3/4	0	0	0	1
7-1/2	1	0	0	1
15	0	1	0	1
30	1	1	0	1
60	0	0	1	1
120	1	0	1	1
300	*	*	*	0

C. To select Deck 1, cause the term DECK 1 to be a binary 1. NOTE: INPUT select is not remotely selectable and must be controlled from front panel in either local or remote operation. To select DECK 2, cause the term DECK 1 to be a binary 0.

D. To select forward operation, cause the term FWD* to be a binary 1. To select reverse operation, cause the term FWD* to be a binary 0.

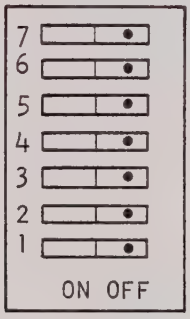
3.2.5 The 9400-610 is now operational.

SECTION IV

ADJUSTMENTS

4.1 OSCILLATOR FREQUENCY ADJUST (Reference Drawing 9400-610)
(This adjustment is accessible through a hole located on the right-hand side of the oscillator.) Used to ad-just the frequency of the 1MHz oscillator to 1MHz ±.01%.

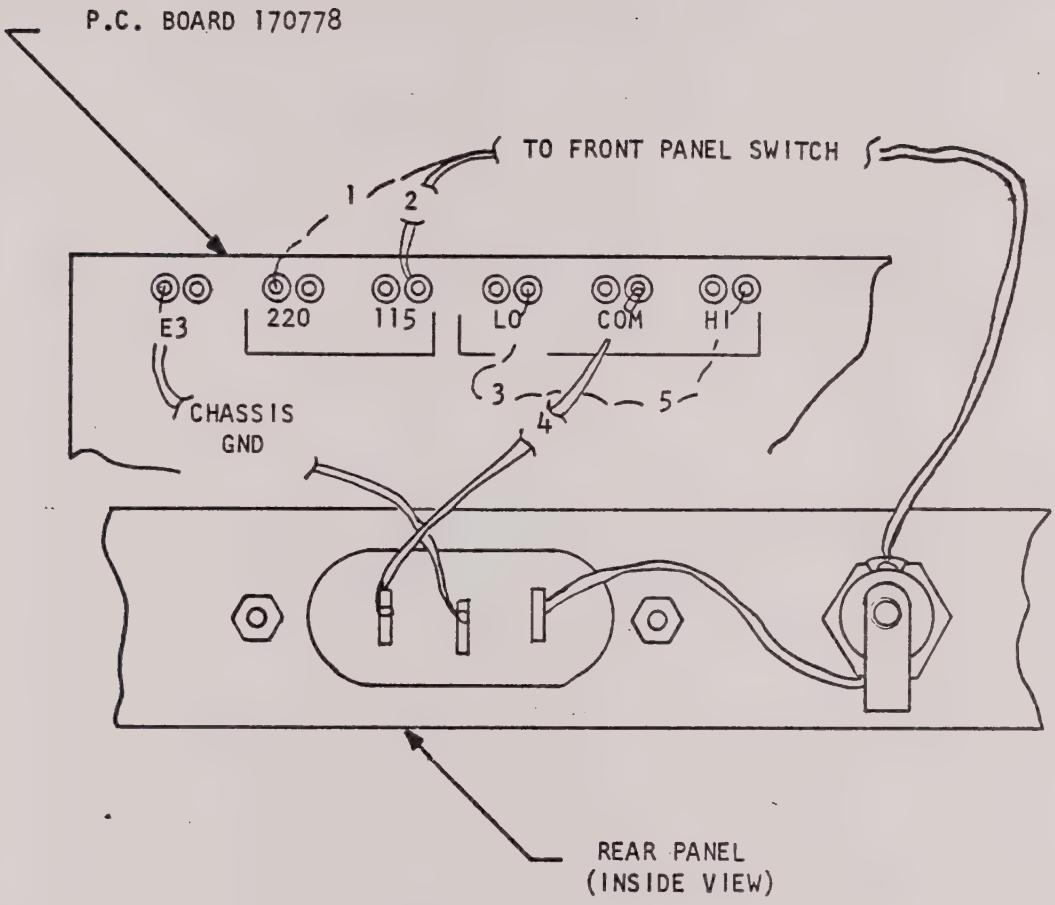
4.2 FRAME BYPASS SELECT (Reference Drawings 9400-610 and 16785 Sheet 8)
Used to select the number of errored time words allowed before the major time counter is corrected to the new time value. Only one position should be selected, otherwise operation of the 9400 will be impaired.



Location A7

4.3 POWER SUPPLY (Reference Drawing 9400-610 and 16280)
R10 adjusts the output level of the +5 volt regulator. Should be set to +5 ±0.25 volts.

NOTE: The Model 9400 is shipped with connections for 115VAC operation unless identified for 230V AC at the AC power connector. See next page for conversion to 230V AC operation.



1. Jumper #1 For 220 VAC Operation
2. Jumper #2 For 115 VAC Operation
3. Jumper #3 For Lo Line Voltage
4. Jumper #4 For Normal Line Voltage
5. Jumper #5 For Hi Line Voltage

SECTION V
THEORY OF OPERATION

5.1 LOGIC DESCRIPTION AND USE

The 9400 is depicted by several drawings. One of these is the top assembly drawing which shows the physical location of the assemblies that are contained within the instrument. This print should be used to locate connectors on the rear panel and for quick reference to the physical location of any of the assemblies or controls.

In the title block of each logic print is a circled number. For instance, the Digital Reader (Minor Time) has circled number (4) in the title block. The Digital Reader (Sync Mode) has circled number (7). The LED display has circled (17) in the title block. Except for terms originating within the drawing being studied, this reference number will precede each term, showing the sheet of logic upon which it originated. To use these numbers, simply observe the term, look at the term reference number in front of the term, then select the print that has this reference number in the title block. This print will show the point of origin of the term you are trying to find. This provides a convenient means of getting back and forth from various pages of these logics.

Each time a term reference number will refer you back to the source of that signal. In each of the logics there will be a number such as A4, A8, A11, etc. These numbers refer to the physical location on this assembly for that particular integrated-circuit element. In order to determine the physical location of an integrated circuit, one would merely refer to the top assembly drawing. In the lower left-hand corner of this drawing, each assembly contained within the instrument is listed, prefixed with a code letter, ((A), (B) etc.) then, by referencing the mechanical view of the top of the instrument, look for the board labeled with that code letter. Examine the board until the desired integrated circuit is located.

5.2 GENERAL LOGIC DESCRIPTION

The DATUM Model 9400 Digital Reader, depicted in block form in Figure 5-1, accepts as its input the Digital Code illustrated in Figure 5-1. The process for decoding this thirty-six bit format is comprised of essentially two steps. The first is one of developing of thirty-six property phased shift register clocks. Once this is accomplished, the data word is shifted into a thirty-six bit shift register. The register outputs are buffered and presented in a parallel form along with appropriate strobe and sample pulses.

Decoding the contents of the time word involves an additional two steps. A seventeen-bit storage register is used to store the seconds-time-of-day contents of the time word. When the function code for Zulu Time is recognized, the contents of the shift register are compared with the contents of the storage register. If the two registers are in disagreement, a strobe pulse is generated which loads the appropriate shift register outputs into the storage register of the major time counter. This load pulse is also used to synchronize the minor time counter which consists of a series of dividers used to derive an IPPS rate update pulse. As long as there is agreement between the shift register and major time counter as each time word is recognized, no strobe pulse is generated, and the major time counter is updated by the IPPS output of the minor time counter.

The contents of the Major Time Counter is converted from straight binary seconds into binary-coded-decimal (BCD) seconds, minutes and hours time-of-day. This BCD information is used to drive a six-digit display and the optional output circuits.

5.3 DETAILED LOGIC DESCRIPTION

This description will be based upon the circled reference numbers contained within the title block of each individual logic print. Before proceeding,

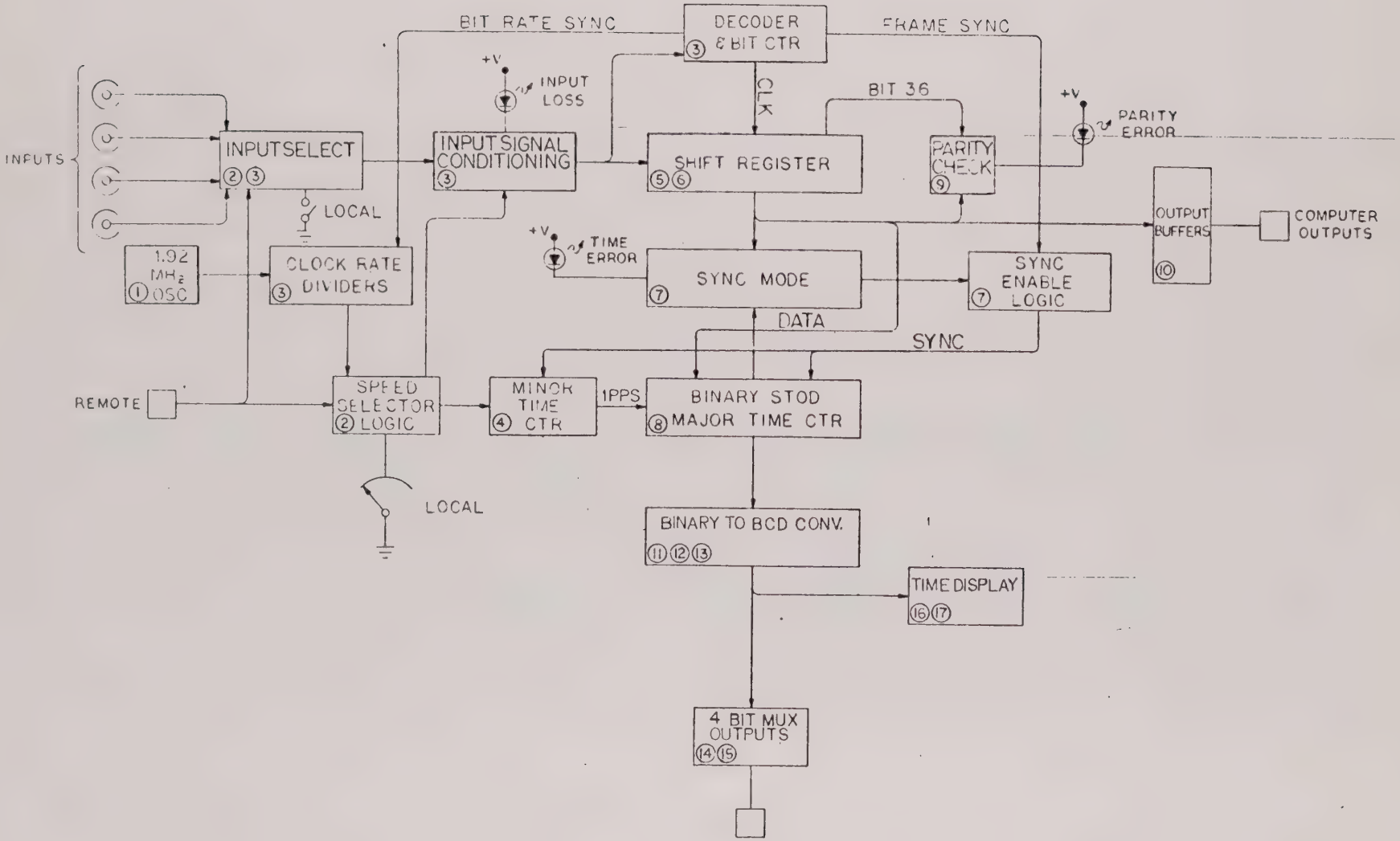
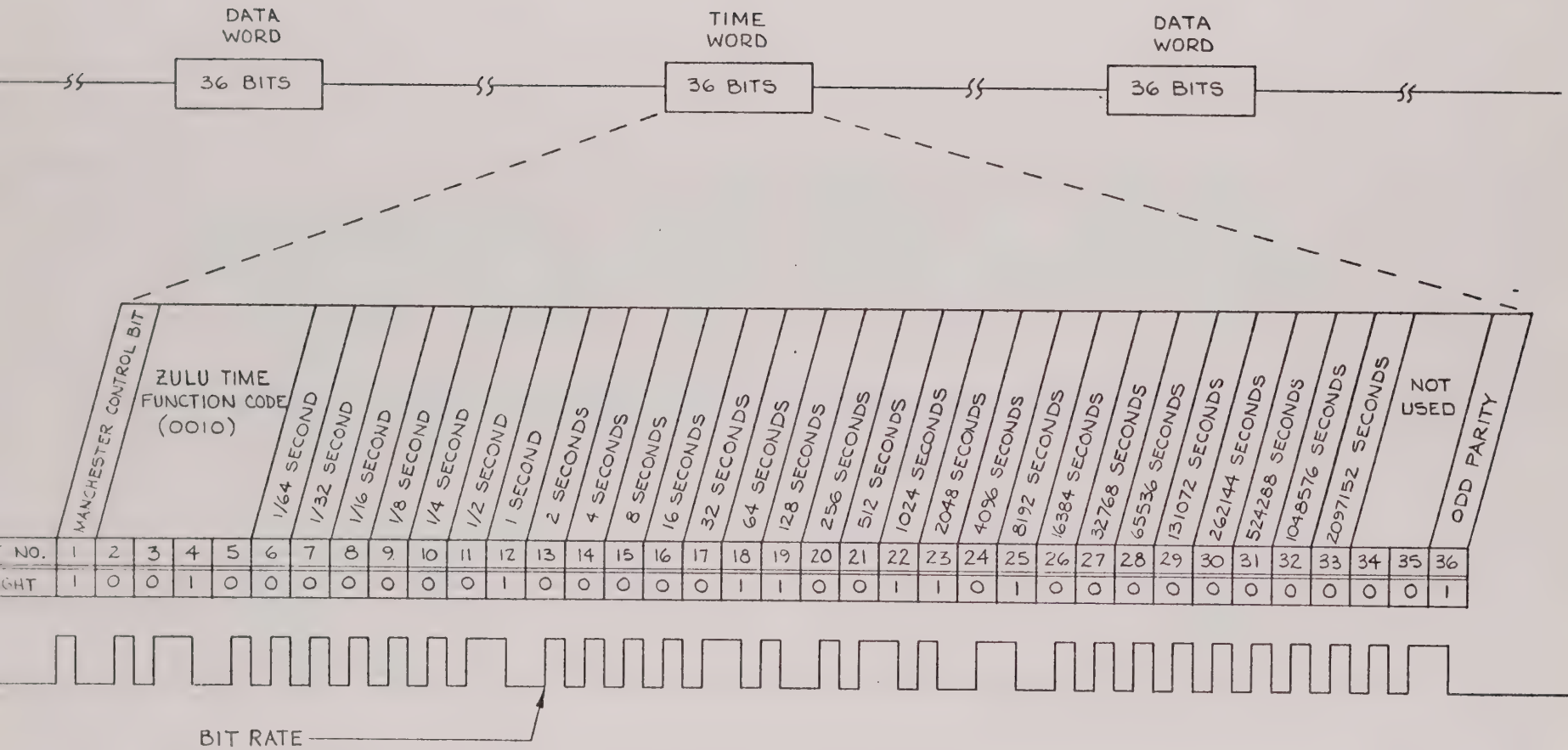

BIT RATE SYNC
DECODER & BIT CTR
FRAME SYNC
+V
INPUT LOSS
CLK
BIT 36
+V
PARITY ERROR
INPUTS
INPUT SELECT
2 3
INPUT SIGNAL CONDITIONING
3
SHIFT REGISTER
5 6
PARITY CHECK
9
OUTPUT BUFFERS
10
COMPUTER OUTPUTS
LOCAL
+V
TIME ERROR
1.92 MHz
1 OSC
CLOCK RATE DIVIDERS
3
SYNC MODE
7
SYNC ENABLE LOGIC
7
DATA
SYNC
REMOTE
SPEED SELECTOR
2 LOGIC
MINOR TIME CTR
4
1PPS
BINARY STOD
8 MAJOR TIME CTR
LOCAL
BINARY TO BCD CONV.
11 12 13
TIME DISPLAY
16 17
4 BIT MUX OUTPUTS
14 15

FIGURE 5-1

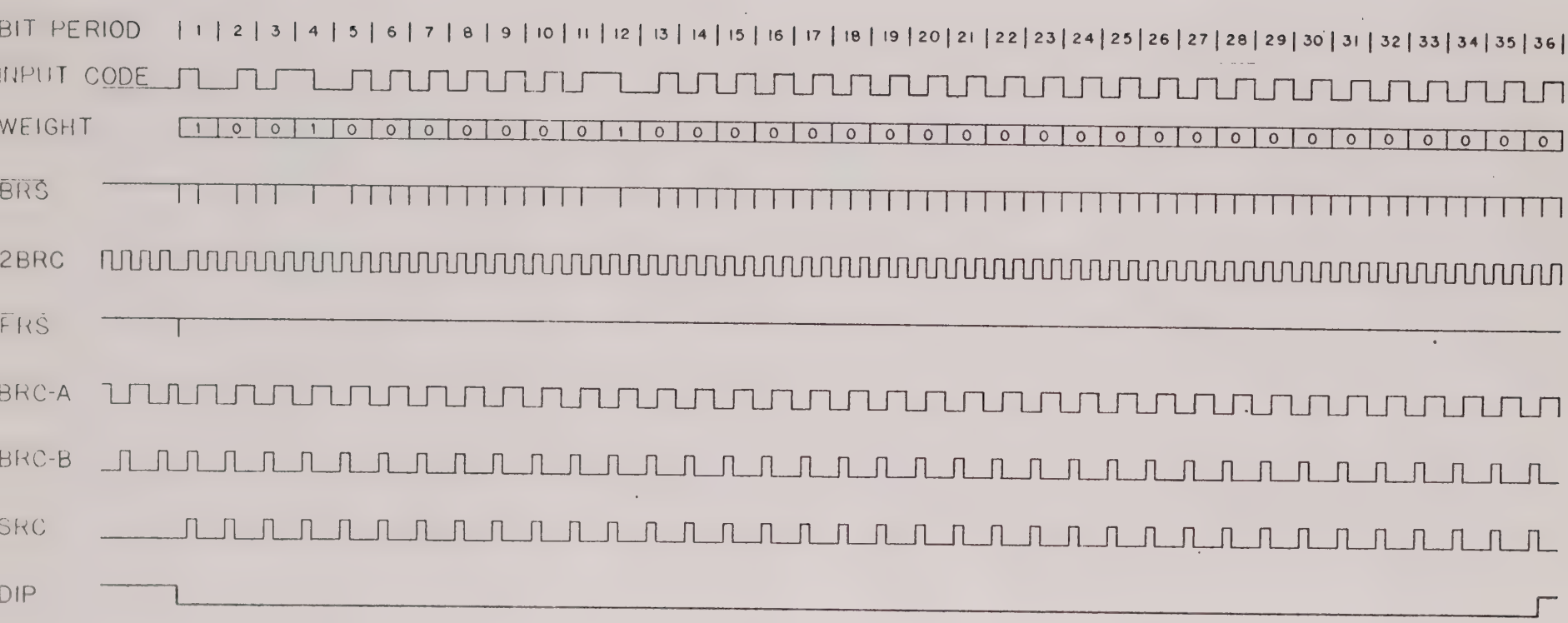


AT:

3 3/4 IPS	3KHz
7 1/2 IPS	6KHz
15 IPS	12KHz
30 IPS	24KHz
60 IPS	48KHz
120 IPS	96KHz
300 IPS	240KHz

TIME DEPICTED IS 11,457 SECONDS/3 HOURS, 10 MINUTES, 57 SECONDS

Figure 5-2.



DIGITAL READER
DECODER TIMING

Figure 5-3.

the reader should be familiar with Paragraph 5.1, LOGIC DESCRIPTION AND USE.

5.3.1 1.92 MHz CLOCK GEN (1)

This logic consists of a 1.92 MHz VCO, which is used as the time base of the 9400, and a 1 MHz crystal oscillator. The output of each is applied to a series of divide-by-five, divide-by-six and divide-by-ten decade dividers. The output of each counter string is an 8 kHz pulse which is applied to a phase comparator. The output of the phase comparator is integrated and used to complete the VCO phase-locked loop.

5.3.2 CLOCK RATE LOGIC (2)

This logic depicts the clock rate generator and the steering logic associated with operating mode operating mode control.

Front panel mode control switches and remote control inputs are routed to two two-way data selectors (A12 and A13). One set of these inputs is selected by operation of the LOCAL/REMOTE CONTROL toggle switch.

The output of the 1.92 MHz VCO, VCO CLK, is routed to a series of binary counters (B15, B16, A16 and A14). The outputs of these counters are routed to an eight-way data selector (A15). One of these outputs, as determined by the desired operating speed, is selected as the clock to the bit-rate clock generator, comprised of flip-flops 2BRC, BRC-A and the gated output, BRC-B.

5.3.3 INPUT LOGIC (3)

This logic contains the input signal conditioning buffers (D18), two decades of bit counters (B18 and C19) and the shift register clock generator (A8).

The selected inputs from Deck 1 and Deck 2 are routed to inverting-type Schmitt buffers. The inverted output of the input selector (ØA) is used to trigger two one-shots, BRS-A and BRS-B to produce sync pulses from both the leading (BRS-A) and trailing (BRS-B) edges of the input code. The OR'ed output of these two pulses ($\overline{\text{BRS}}$) provides the bit rate sync pulses used to sync the clock rate counter on (2) which have duty cycles less than the period of the selected bit rate.

Bit rate clock BRC-B is used as the shift register clock (SRC*). Bit rate clock BRC-A is routed to decade dividers B18 and C19. When thirty-five BRC-A's have been counted, the trailing edge of the next BRC-B clocks the Data In Place flip-flop DIP true, inhibiting any further shift register clocks. On the fortieth clock, BC 40 goes true, inhibiting further counting and enabling the leading edge of the first bit of the next word to generate the frame rate sync pulse (FRS) which resets the two counters and the bit rate clock generator BRC-A on (2) .

The two "exclusive - OR" elements associated with the POLARITY switch assure that the data being presented to the shift register is of the proper polarity in both forward and reverse operation.

Also contained on this logic print is the activity sensor TN which is set for approximately one-half second. If the input code is lost or is there is more than one-half second between data words, TN "times out", the INPUT LOSS alarm indicator is illuminated and the clock rate counters (B15 and B16) on (2) are inhibited by the term $\overline{\text{STOP}}$.

5.3.4 MINOR TIME COUNTER (4)

This logic consists of a divide-by-six and three divide-by-ten decimal counter units (DCU) which divide the bit rate clock BRC-A by six thousand to produce a series of scan terms and tsc8 (1pps at 7-1/2 ips), which is used to update the major time counter (8) . The counters are synchronized each time word by the term $\overline{\text{REC1}}$ from the Sync Mode Logic (7) .

Additionally, this logic generates the Data Ready Pulse (DRP) and the Output Strobe Pulse (OSP). The leading edge of the Data In Place Pulse ($\overline{\text{DIP}}$) clocks the Data Enable Pulse flip-flop true, enabling DRP. The next MCC pulse clocks DRP true, enabling OSP. The following MCC pulse clock DRP and OSP false. Thus DRP is a two microsecond wide pulse which begins one microsecond or less after the data is in place and OSP is a one microsecond wide pulse occurring one microsecond after DRP.

5.3.5 SHIFT REGISTER (5) (6)

This logic consists of two thirty-six bit shift registers plus directional and clock steering logic. The shift register on (5) is a bi-directional shift register. In the forward direction, data enters at H3, Pin 7 and is shifted left toward H6, Pin 15 by the SL enable and SRC clocks. In reverse operation, data is entered at H6, Pin 2 and is shifted right toward H3, Pin 12 by the SR enable and the SRC clocks. At the completion of the thirty-six shifts, the data present at H6, Pin 15 (SR01) represents the Manchester Control Bit which is always a binary "one".

The shift register on (6) is a shift right register used to assure the proper phase releationship in reverse operation. In this operating mode, the outputs of this register represent the complement of the outputs of the Bi-directional shift register (5). At the conclusion of the shift cycle, if SR01 is a binary "zero", the contents of the shift register (6) is parallel-loaded into shift register (5) by an extra SRC clock generated via C18-11.

5.3.6 SYNC MODE (7)

This logic consists of a series of four-bit data comparators (J4-J8) and associated logic used to recognize the receipt of a time word and to strobe the time data into the Major Time Counter (8).

When data is in place (i.e., DIP is true), shift register outputs SR02-SR05 are examined by J6 for presence of the Zulu Time function code 0010. Each time this function code is recognized, shift register outputs SR12-SR28 are compared with the contents of the major time counter $S2^{0}$-$S2^{16}$. If the two registers are not in agreement, error detector ECD clocks true. A few microseconds later ECD is reset, incrementing binary counter B7. Each errored time word causes B7 to be incremented by one count. When the selected number of errored time words have beem counted (as determined by the setting of switch assembly A7), the term SEC (Selected Error Count) clocks true. Upon receipt of the next time word, flop-flop REC1 generates the data load pulse ($\overline{DLP}$) which loads SR12-SR28 into the major time counter (8). When the following time word is received, the contents of the major time counter and

the shift register should now agree. ECD remains reset, allowing the error counter B7 to be reset by $\overline{REC}$. Note that once the selected error count is reached, further clocking of the error counter is inhibited by SEC. Note also that the error counter can be reset only when no error exists.

Each time an error is detected, flip-flop EDS is set, illuminating the TIME ERROR alarm indicator. When the error is cleared, EDS is reset.

5.3.7 MAJOR TIME COUNTER (8)

This logic consists of a series of binary up/down counters (C1-C5) used to accumumate the contents of the time word in seventeen bits of binary seconds. The counters are initially preset with the time word contents by the term $\overline{DLP}$ from the sync mode logic (7). The counter is subsequently incremented or decremented by one-shot 1PPS CLK.

Twenty-four-hour radix is accomplished by using a series of four-bit data comparators B1-B5 and one-shots RCP1 and RCP2. In the forward direction these comparators are programmed to look for a binary count of 0000000110001-0101, which corresponds to a time of 24 hours, 00 minutes, 00 seconds, or midnight. Reaching equality enables RCP1 which is then triggered one microsecond later by the trailing edge of 1PPS CLK. This in turn triggers RCP2 which, in the forward direction, generates the term FZS which resets the up/down counters to zero.

In reverse, the comparators are programmed to look for all binary ones. (This occurs on the next "down" clock after the counters have reached zero.) One microsecond later, RCP2 resets the binary counters to 24 hours, 00 minutes and 00 seconds. Five microseconds later, RCP1 "times out", generating an additional 1PPS CLK, which decrements the counter to a count of 23 hours, 59 minutes, and 59 seconds.

5.3.8 PARITY ERROR DETECTOR (9)

This logic consists of a series of parity checkers which examine shift register outputs SR01-SR35 to derermine odd or even parity. The output is compared with parity bit, SR36 in B11-11. If there is disagreement, strobe

pulse OSP clocks the parity error detector flip-flop PED true, illuminating the PARITY ERROR alarm indicator.

5.3.9 DATA OUTPUT BUFFERS (10)

This logic provides thirty-two parallel bits of buffered data outputs from the Shift Register (5) . In addition, TTL indications of the three alarm conditions are provided, along with a two microsecond Data Ready Pulse and a one microsecond Output Strobe Pulse at the conclusion of each word.

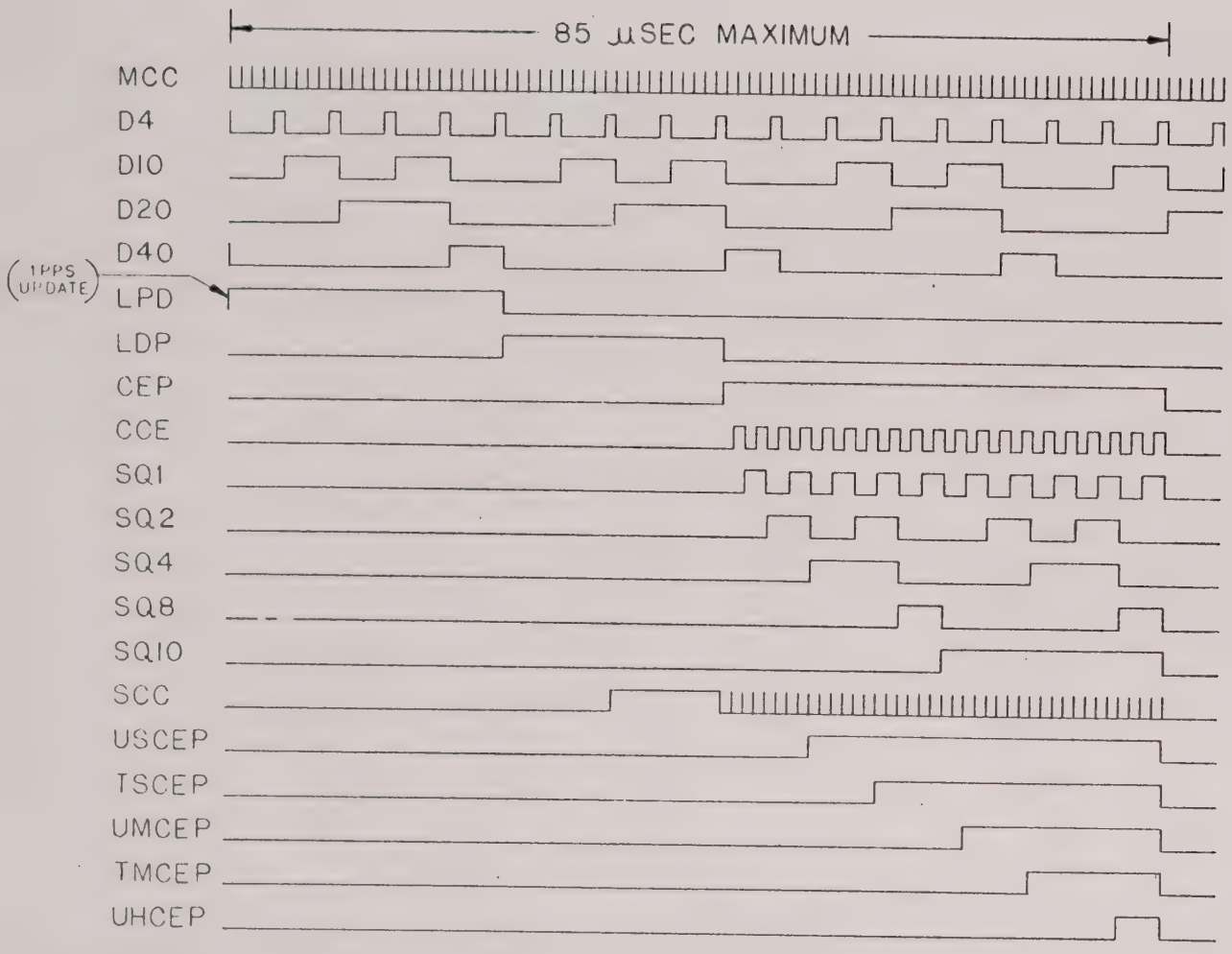
5.3.10 BINARY-TO-BCD CONVERTER (11) (12) (13)

This logic converts the seventeen-bit binary time-of-day outputs into a twenty-bit, binary-coded-decimal (BCD) 8-4-2-1 format, representing time-of-day in seconds, minutes and hours. The conversion process is accomplished by a series of four-bit shift registers (F1-F5); two-way, four-bit data selectors (D1-D5); four-bit full adders (E1-E5); and associated timing and steering logic elements. The following is a step-by-step explanation of the conversion process. Refer to Figure 5-4 for converter timing.

Conversion is initiated with the 1PPS update clock (tsc8) from the minor time counter (4) . Within thirty-five microseconds after update (actual time is determined by the relationship of update time to clock pulse D40 from (1)), the contents of the major time counter is loaded through the data selectors into the shift registers. The shift register outputs are routed to the four-bit adders.

Eleven microseconds later, the adder outputs are loaded into the shift registers with the leading edge of clock SCC. The next leading edge of SCC shifts the data one bit to the right. The next SCC loads the updated adder outputs into the shift register, which is again shifted one bit by the next SCC. After four of these "load/shift" cycles, the Unit Seconds data outputs of F1 are examined. If the result is five or more, three seconds are added to the existing count.

Three more "load/shift" cycles are performed. The Tens of Seconds data outputs of F2 are examined. If the result is thirty or more, ten seconds are added to the existing count.



BINARY TO BCD CONVERTER
TIMING DIAGRAM

Figure 5-4.

The remainder of the conversion process is similar to that for Unit Seconds and Tens of Seconds, with four "load/shift" cycles for Unit Minutes, three for Tens of Minutes, four for Unit Hours and two for Tens of Hours. The entire conversion process requires from sixty to eighty-five microseconds, again depending upon when update occurs in relationship to clock pulse D40.

5.3.11 I/O CONTROL (14)

This logic consists of four data multiplexers (K1-K4) which take the twenty outputs of the binary-to-BCD converter (13) and multiplex them into four data lines representing BCD 1, 2, 4 and 8. Fifty-microsecond periods are assigned successively to Unit Seconds, Tens of Seconds, Unit Minutes, Tens of Minutes, Unit Hours and Tens of Hours. Timing is determined by scan terms LC1, LC2, LC4 and LC8 from the Output Mux Scan logic (15) .

Also depicted on this logic are the remote control inputs. SPC1, SPC2 and SPC4 are the remote speed control inputs. $\overline{\text{ESS}}$ is the remote search speed command which, when activated, overrides SPC1, SPC2 and SPC4, causing all three to become a binary one.

5.3.12 OUTPUT MUX SCAN (15)

This logic is used to generate six twenty-five-microsecond wide strobe pulses and four scan terms used for controlling the multiplexers on the I/O Control logic (14) .

Flip-flop MC1 divides the 80 kHz clock D10 to produce a 40 kHz squarewave which clocks flip-flop MC2 which is normally held reset. Two milliseconds after the 1PPS update, flip-flop SCG clocks true, allowing MC2 to toggle. The fifty-microsecond periods of MC2 are counted by divide-by-ten counter M2. The BCD outputs of this counter are routed to the four multiplexers on (14) and to four-to-ten line converter M1. The output of M1 is a series of six sequential twenty-five-microsecond wide strobe pulses used by the Model 9300-713 for loading the four lines of BCD data from K1-K4 on (14) . When counter M2 reaches a count of eight, this triggers one-shot RST which resets SCG which, in turn, resets MC2.

SCG is inverted and provided as the tape search enable pulse TSEP* which is true except for the four hundred microseconds required for the output multiplexing operation.

$\overline{\text{FRATE}}$* is a frame rate pulse which is normally binary one and becomes a binary zero for two milliseconds following the 1PPS update (tsc8). This pulse is inhibited by $\overline{\text{EDS}}$ during time words in which there is a detected time error.

5.3.13 LED DISPLAY (DRIVERS) (16)

This logic consists of six BCD-to-seven-segment decoder/drivers which convert the BCD time-of-day outputs from (13) into the seven-segment form required by the LED display.

5.3.14 LED DISPLAY (17)

This logic consists of six light emitting diode type display elements which convert the seven-segment outputs from (16) into a visual display representing decoded time-of-day in seconds, minutes and hours.

5.3.15 POWER SUPPLY (49)

This Power Supply furnishes regulated $\pm$15V DC and +5V DC to the unit. The $\pm$15V DC regulators (A2 and A3) are integrated circuit regulators with internal over-current protection. The +5V DC regulator employs an LM305 voltage regulator and is of the switching type.

The LM305 is essentially an operational amplifier with a built-in Zener reference. When the voltage on pin 6 falls a few millivolts below that of the internal reference, Q1 and Q2 are turned on and the voltage on the 5 volt line begins to rise. Q1 and Q2 turn off as the voltage on A1-6 rises above the reference level. L1 tries to maintain constant current flow and current begins to flow through CR2. This continues until Q1 and Q2 are again turned on and the cycle is repeated.

The switching regulator is thus an efficient method of obtaining constant 5V DC from an unregulated source, since power is dissipated in Q1 only when it is on or changing states.

For 5 volts from a 23V source, Q1 is on approximately 25% of the time. Q3 and Q4 provide short circuit protection by forcing the regulator to decrease the output voltage when the current through R7 becomes excessive. When the output voltage becomes too high, CR5 conducts and CR6 is turned on. The current limit circuit then shuts down the regulator.

SECTION VI
MAINTENANCE

The 9400 Digital Reader utilizes integrated circuits. There are no moving parts or parts with limited life. There is no periodic maintenance required for the unit under normal conditions. If the unit is exposed to unusual operating conditions such as high dust or high humidity environments, or if the unit is dropped or otherwise damaged, it may be necessary to perform certain inspections and/or repairs.

WARNING

115 or 220V AC is present in the unit's power supply. Use caution at all times when operating with power on and the protective cover removed.

If it is necessary to inspect the unit, the following should be considered:

1. Always disconnect AC power before removing the instrument cover. To remove the cover, simply remove the screw at the rear panel and slide the cover off to the rear.

2. Make a thorough visual inspection of all circuitry and wiring.

3. Check for physical integrity of all components. Look for burned or cracked components, loose physical damage, leakage of insulation compounds or general physical damage. To aid in overall maintenance and repair, each integrated circuit is mounted in an individual modular socket. Removal or replacement is therefore convenient and easy.

   It should rarely be necessary to replace an integrated circuit; however, if replacement is attempted, be sure that all component leads enter the socket and that no leads are bent under the component or extended out from the socket.

Check to see that all IC's are firmly mounted in the socket so that good electrical contact is made.

4. Check all switches and connectors for loose or broken wires.

5. If the internal component surfaces and components have an excessive amount of dust deposited on them, use a soft brush and a low pressure stream of air to remove any foreign material.

CAUTION

Do not clean PC boards or small internal components with a stiff brush or solvents since damage to the circuits may result. A high powered vacuum cleaner device should not be used on small internal components.

6. Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints and other foreign material.

7. Replace the cover and reconnect the AC power and input connector. Check operation. If performance does not match or exceed the specifications listed in Section II corrective maintenance is in order.

Printed Circuit Board Repair

Removal and insertion of IC components can be easily made as described above. Should it be necessary to replace conventional components which are soldered to the circuit board, cut the leads of the part near the lead holes. Using a low power (50 watts or less) soldering iron, apply heat sparingly to each cut lead. As soon as the solder melts, slip the lead from the hole and clean the hole with a tooth pick. Clean the board surfaces with isopropyl alcohol. Form the tinned leads of the replacement part and insert in cleaned holes, trimming the leads to extend 1/16-inch beyond the back surface of the board. Only 63/37 solder with a maximum diameter of 1/6 inch should be used. Solder the leads to the board and use a hemostat, long nosed pliers, or other heat sink on the leads of all semiconductor devices and quarter-watt resistors. Allow the soldered junction to cool before removing the heat sink.

SECTION VII

CONNECTOR PIN ASSIGNMENTS

DATA OUTPUTS, J6 (Drawing 16785, Sheet 11)

Pin	Term	Pin	Term
1	DB2	21	DB22
2	DB3	22	DB23
3	DB4	23	DB24
4	DB5	24	DB25
5	DB6	25	DB26
6	DB7	26	DB27
7	DB8	27	DB28
8	DB9	28	DB29
9	DB10	29	DB30
10	DB11	30	DB31
11	DB12	31	DB32
12	DB13	32	DB33
13	DB14	33	DATA READY
14	DB15	34	OUTPUT STROBE
15	DB16	35	INPUT LOSS
16	DB17	36	TIME ERROR
17	DB18	37	PARITY ERROR
18	DB19	38-48	NOT USED
19	DB20	49	GROUND
20	DB21	50	GROUND

I/O CONTROL, J5 (Drawing 16785, Sheets 15, 16)

Pin	Term	Pin	Term
1	$\overline{\text{SET US}}$	11	$\overline{\text{FRATE*}}$
2	$\overline{\text{SET TS}}$	12	GO
3	$\overline{\text{SET UM}}$	13	$\overline{\text{ESS}}$
4	$\overline{\text{SET TM}}$	14	FWD*
5	$\overline{\text{SET UH}}$	15	DECK 1
6	$\overline{\text{SET TH}}$	16	SPC 1
7	BCD 1	17	SPC 2
8	BCD 2	18	SPC 4
9	BCD 4	19-22	GROUND
10	BCD 8	23	TSEP*

SECTION VIII

LIST OF MATERIALS

8.1 INTRODUCTION

This section contains a list of materials for each assembly. The unit materials list contains a list of all major assemblies and any parts that are not located on one of the major assemblies.

Each major assembly's materials list contains a list of all components used in the construction of that particular assembly.

8.2 MATERIALS LIST

Digital Reader Top Assembly	9400-610
Power Supply Assembly	16280-3
Digital Reader P.C. Board Assembly	16785
LED Display Assembly	16832

MATERIAL LIST

Date	Drawn	Title	Assy No.	Sheet	REV
8-15-75	CARY	DIGITAL READER	9400-610	1 of 2	

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY	REF. DESIGNATION
1	1202-0102	SWITCH SPDT	DATUM	7	
2	1206-1020	SWITCH BCD	DATUM	1	
3	1704-1002	RECEPT BNC	DATUM	4	
4					
5	1708-1252	SKT	DATUM	1	
6	1795-0001	WASHER	DATUM	4	
7	1795-0002	WASHER	DATUM	4	
8	2204-0005	LED INDIC	DATUM	3	
9	2310-4000	SPACER	DATUM	1	
10	2310-1300-09	STANDOFF	DATUM	1	
11	2325-0051	CLIP	DATUM	1	
12	2325-2005	FASTENER	DATUM	2	
13	2524-7020	KNOB	DATUM	1	
14	507-4537-1437-640	LAMP	DIALCO	1	
15					
16	700364-2	COVER STK	DATUM	2	
17					
18	704757-2	SIDE GUSSET STK	DATUM	2	
19	705378	MTG BKT	DATUM	2	
20	705503-1	FRONT PANEL	DATUM	1	
21	705504-1	COVER PLATE	DATUM	1	
22	705505	LENS	DATUM	1	

MATERIAL LIST

Date	Drawn	Title	Assy No.	Sheet	REV
8-15-75	CARY	DIGITAL READER	9400-610	2 of 2	

ITEM	STOCK/PART NO.	DESCRIPTION		MFR/SPEC	QTY	REF. DESIGNATION
23	705506	REAR PANEL		DATUM	1	
24	705616	CENTER SUPPORT		DATUM	1	
25						
26	931500	HANDLE	STK	DATUM	2	
27	16280-3	POWER SUPPLY	STK	DATUM	1	
28	16785	DIGITAL READER		DATUM	1	
29	16832	DISPLAY		DATUM	1	
30						
31	SK9400-610	SHIPPING KIT		DATUM	1	
32						
33	803963	WIRE LIST		DATUM	REF	

DATE: 11-14-74
DRAWN: GME
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:

REV B

TITLE: POWER SUPPLY +5V I 15V

ASS'Y NO: 16280-3

SHT 1 OF 3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	0102-0220	RESISTOR 22Ω ¼W 5%	DATUM	1	R4		
2	" -0680	" 68Ω " "	"	2	R2,12		
3	" -0101	" 100Ω " "	"	1	R13		
4	" -0332	" 3.3K " "	"	1	R11		
5	" -0472	" 4.7K " "	"	1	R1		
6	" -0682	" 6.8K " "	"	1	R9		
7	" -0473	" 47K " "	"	2	R5,6		
8	" -0754	" 750K " "	"	1	R3		
9	0125-0R10	" .1Ω 3W	"	1	R7		
10	0154-1001	" POT 1K	"	1	R10		
11							
12	0212-0223	CAPACITOR .022μf 100V	"	1	C6		
13	0219-0588	" 5800μf 40V	"	1	C1		
14	0220-0475	" 4.7μf 35V	"	3	C8,10,11		
15	" -0476	" 47μf 35V	"	1	C9		
16	" -0476-2	" " 20V	"	1	C4		
17	0226-0103	" .01μf 1000V	"	2	C101,102		
18	" -0104	" .1μf 10V	"	2	C5,7		
19							
20	0301-7815	IC UGH7815393	"	1	A3		
21	" -9305	" LM305	"	1	A1		
22	" -9320	" LM320-15H	"	1	A2		
23							
24	0500-0336	DIODE 1N914A	"	1	CR3		
25	0515-0752-1	" 1N752A	"	1	CR5		
26	0540-0106-1	" MCR106-1	"	1	CR6		

NOTES:

DATE: 11-14-74
DRAWN: QAE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:

REV B

TITLE: POWER SUPPLY +5V, ±15V

ASS'Y NO: 16280-3

SHT 2 OF 3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
27	0540-0447	BRIDGE RECT VS447	DATUM	1	CR51		
28	" -0820	DIODE MR820	"	1	CR2		
29	" -4720-1	" IN4720	"	1	CR1		
30	" -4934	" IN4934	"	2	CR7,8		
31							
32	0550-035A	TRANSISTOR TIP-35A	"	1	Q1		
33	" -7705	" 2N3565	"	1	Q4		
34	0555-6005	" 2N2905A	"	1	Q2		
35	" -6600	" 2N3645	"	1	Q3		
36							
37	0601-6045	CHOKE	"	1	L1		
38	" -6082	TRANSFORMER	"	1	T1		
39							
40	0702-0010	FUSE 1A S/B 3AG	"	1	F1		
41							
42	0750-0200	" HOLDER	"	1	XF1		
43							
44	1704-1061-1	CONNECTOR AC	"	1			
45							
46	1706-0033	EYELET	"	2	(L1)		
47	1708-3897	SOCKET 14P W/W	"	1			
48	" -8000	" 8P	"	1	XA1		
49							
50							
51	2310-1247-09	STANDOFF	"	1	(L1)		
52	2325-1004	TOROID RETAINER	"	2	(L1)		

NOTES:

DATE: 11-14-74
DRAWN: GHE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:

REV B

TITLE: POWER SUPPLY +5V, ±15V

ASS'Y NO: 16280-3

SHT 3 OF 3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
53	704561	MTG PLATE STK	DATUM	1			
54	704562	SIDE BRKT STK	"	1			
55	704563	HEATSINK STK	"	1			
56	704966-1	MTG BRKT STK	"	1			
57	704966-2	" "	"	2			
58							
59	170778	PC BOARD STK	"	1			
60	170779	" " STK	"	1			

NOTES:

MATERIAL LIST

Date	Drawn	Title	Assy No.	Sheet	REV
8-15-75	R. FLOCK	DIGITAL READER	16785	1 of 4	

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY	REF. DESIGNATION
1	0102-0100	RESISTOR, 10Ω , 1/4W, 5%	DATUM	1	R5
2	0102-0511	RESISTOR, 510Ω, 1/4W, 5%	DATUM	5	R1, 2, 38, 41, 46
3	0102-0102	RESISTOR, 1K, 1/4W, 5%	DATUM	5	R4, 7, 40, 47, 48
4	0102-0562	RESISTOR, 5.6K, 1/4W, 5%	DATUM	9	R8-13, 39, 42, 44
5	0102-0103	RESISTOR, 10K, 1/4W, 5%	DATUM	7	R35, 36, 43-45,50,51
6	0102-0153	RESISTOR, 15K, 1/4W, 5%	DATUM	1	R37
7	0102-0104	RESISTOR, 100K, 1/4W, 5%	DATUM	1	R3
8	0225-0152	CAPACITOR, 1500pf 100V	DATUM	1	C48
9	0212-0152	CAPACITOR .0015µf @ 100V	DATUM	1	C14
10	0220-0105	CAPACITOR 1µf @ 35V	DATUM	4	C8, 12, 16, 17
11	0220-0475	CAPACITOR 4.7µf @ 35V	DATUM	17	C1,2,7,20,23,24,
--					27,28,31,32,35,36,
--					39,40,42,45,46
12	0220-0106-1	CAPACITOR 10µf @ 35V	DATUM	1	C3
13	0220-0476-1	CAPACITOR 47µf @ 6V	DATUM	1	C4
14	0220-0107	CAPACITOR 100µf @ 10V	DATUM	1	C11
15	0225-0330	CAPACITOR 33pf @ 100V	DATUM	3	C9, 10, 19
16	0225-0101	CAPACITOR 100pf @ 100V	DATUM	1	C6
17	0225-0331	CAPACITOR 330pf @ 100V	DATUM	2	C13, 18
18	0225-0561	CAPACITOR 560pf @ 100V	DATUM	1	C15
19	0226-0103-1	CAPACITOR .01µf @ 50V	DATUM	1	C5
20	0226-0104	CAPACITOR .1µf @ 10V	DATUM	14	C21,22,25,26,29,30,33, 34,37,38,41,43,44,47

MATERIAL LIST

Date	Drawn	Title	Assy No.	Sheet	REV
8-15-75	R. FLOCK	DIGITAL READER	16785	2 of 4	

ITEM	STOCK/PART NO.	DESCRIPTION		MFR/SPEC	QTY	REF. DESIGNATION
21	0301-4024	I.C.	MC4024P	DATUM	1	C14
22	0301-4044	I.C.	MC4044P	DATUM	1	C13
23						
24	0301-7H03	I.C.	SN74H103N	DATUM	11	A4,5,17,C10,D6,7,9
--						E8,F9,L2,3
25	0301-7L85	I.C.	SN74L85	DATUM	11	B1,2,3,4,5, J4,5,
--						6,7,8,9
26	0301-7123	I.C.	SN74123N	DATUM	4	A3,19, C16, L4
27	0301-7151	I.C.	SN74151N	DATUM	5	A14, K1,2,3,4
28	0301-7157	I.C.	SN74157	DATUM	7	A12,13, D1,2,3,4,5
29	N74180A	I.C.		SIGNETICS	5	K5,6,7,8,9
30	0301-7193	I.C.	N74193	DATUM	5	C1,2,3,4,5
31	0301-7194	I.C.	SN74194	DATUM	14	F1,2,3,4,5, H1,2,3,
--						4,5,6,7,8,9
32	0301-7400	I.C.	N7400A	DATUM	5	A1,6, C17, L1, M3
33	0301-7404	I.C.	N7404A	DATUM	2	B17, C7
34	0301-7408	I.C.	USN7408A	DATUM	19	A2,8, C6,18, D19, E6,
--						7, F8, J2, L5,6,7,8,
--						9, M5,6,7,8,9
35	0301-7413	I.C.	SN7413	DATUM	1	D18
36	0301-7420	I.C.	N7420A	DATUM	1	B19
37	0301-7432	I.C.	N7432A	DATUM	6	A18, B6, F6,7,J3,M4

MATERIAL LIST

Date	Drawn	Title	Assy No.	Sheet	REV
8-15-75	R. FLOCK	DIGITAL READER	16785	3 of 4	

ITEM	STOCK/PART NO.	DESCRIPTION		MFR/SPEC	QTY	REF. DESIGNATION
38	0301-7442	I.C.	N7442	DATUM	1	M1
39	0301-7473	I.C.	N7473A	DATUM	2	A14,16
40	0301-7474	I.C.	SN7474	DATUM	2	A11, B8
41	0301-7483	I.C.	SN7483	DATUM	5	E1,2,3,4,5
42	0301-7486	I.C.	N7486	DATUM	1	B11
43	0301-7805	I.C.	FμGH7805393	DATUM	1	D16
44	N8273B	I.C.		SIGNETICS	4	C8,9, E9, J1
45	0301-8280	I.C.	N8280A	DATUM	13	A9,10, B7,9,12,15,
--						18, C11,15,19, D8,17
--						M2
46	0301-8281	I.C.	N8281A	DATUM	2	B13, B16
47	0301-8288	I.C.	N8288A	DATUM	2	B10, B14
48						
49						
50	0550-7705	TRANSISTOR	2N3565	DATUM	1	Q1
51	1202-5166-1	SWITCH	PIANO	DATUM	1	A7
52	1301-0001	OSCILLATOR		DATUM	1	Y1
53	1704-0024	RECEPT	24P	DATUM	1	
54	1704-0050	RECEPT	50P	DATUM	1	
55						
56	1708-3897	SKT. 14P	W/W	DATUM	74	
57	1708-3898	SKT. 16P	W/W	DATUM	57	

MATERIAL LIST

Date	Drawn	Title	Assy No.	Sheet	REV
8-15-75	R. FLOCK	DIGITAL READER	16785	4 of 4	

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY	REF. DESIGNATION
58					
59	705507	CONN PLATE	DATUM	1	
60					
61					
62	171165A	P.C. BOARD	DATUM	1	

MATERIAL LIST

Date	Drawn	Title	Assy No.	Sheet	REV
6-4-75	R. FLOCK	DISPLAY	16832	1 of 1	

ITEM	STOCK/PART NO.	DESCRIPTION		MFR/SPEC	QTY	REF. DESIGNATION
1	0102-0102	RESISTOR, 1K, 1/4W, 5%		DATUM	1	R1
2						
3	0220-0475	CAPACITOR 4.7µf @ 35V		DATUM	1	C1
4						
5	0301-9374	I.C.	9374DC	DATUM	6	A2 - A7
6						
7	1708-0036	HEADER		DATUM	2	
8	1708-3788	SKT		DATUM	6	DS2 - DS7
9	1708-3898	SKT		DATUM	6	A2 - A7
10						
11	2205-0005	NUM INDIC		DATUM	6	DS2 - DS7
12						
13	2310-1591-B	MTG BLOCK		DATUM	2	
14						
15	170937	P.C. BD.	STK	DATUM	1	
16	171126	P.C. BD.	STK	DATUM	1	

MATERIAL LIST

Date	Drawn	Title	Assy No.	Sheet	REV
6-4-75	R. FLOCK	SHIPPING KIT	SK9400-610	1 of 1	

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY	REF. DESIGNATION
1	1704-0024-1	PLUG 24P	DATUM	1	
2					
3	1704-0050-1	PLUG 50P	DATUM	1	
4					
5	4000-2004	POWER CORD	DATUM	1	

SECTION IX

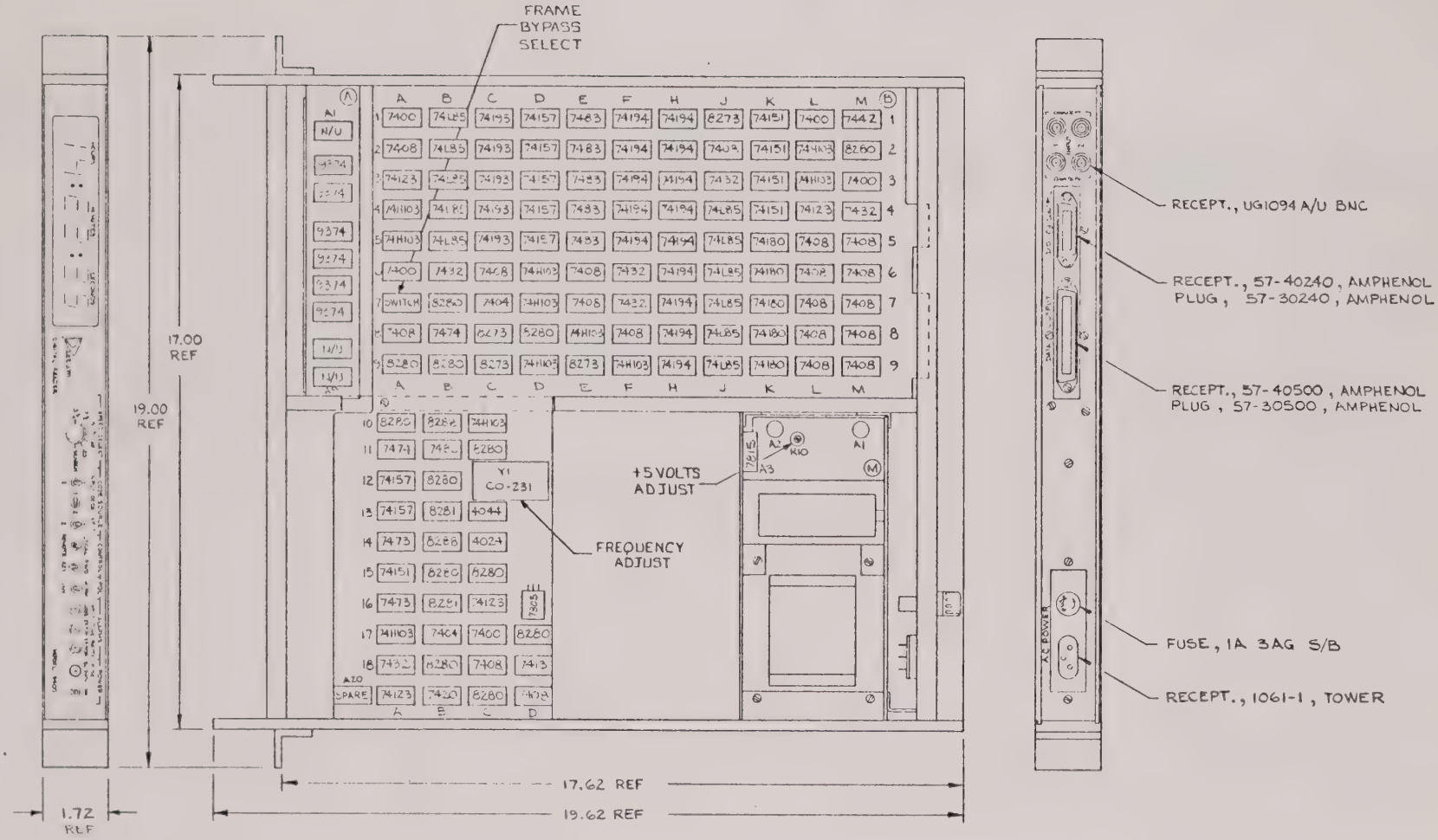
DRAWINGS

9.1 INTRODUCTION

This section contains the drawings which are applicable to the Digital Reader. In most cases, the schematics are used as logic drawings which not only enable one to locate particular elements but also to trace signals from one schematic to another. Each logic drawing (schematic) has a circled number in its title block and are filed in this order.

9.2 DRAWING LIST

Digital Reader	9400-610
Digital Reader (1) - (15)	16785
LED Display (16) (17)	16832
Power Supply (49)	16280



3. SLIDES AND REAR MTG BRACKETS ARE OPTIONAL

Ⓜ 16280-3 POWER SUPPLY ASSY.
Ⓑ 16785 DIGITAL READER ASSY.

2. Ⓐ 16852 LED DISPLAY

1. TOP COVER REMOVED FOR CLARITY

NOTES: UNLESS OTHERWISE SPECIFIED

5. UNIT WIRE LIST 803963
J7 - AC POWER INPUT
J6 - DATA OUTPUT
J5 - I/O CONTROL
J4 - DECK 2 INPUT 1
J3 - DECK 2 INPUT 2
J2 - DECK 1 INPUT 1
4. J1 - DECK 1 INPUT 2

THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT

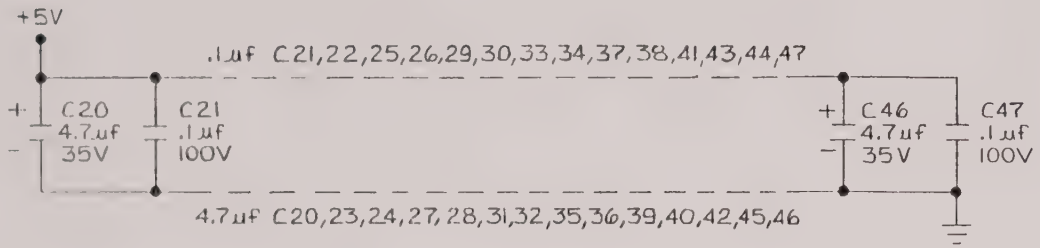
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL. .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

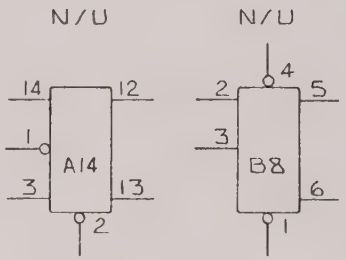
TITLE: DIGITAL READER

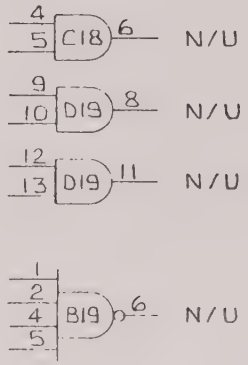
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

DWN MILES | CHK | DES | ENGR | SCALE HALF | FSC 32160 | SIZE C | 9400-610 | SHT 1 OF 1 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED







N7400	A1, A6, C17, L1, M3	N74123	A3, A19, C16, L4
N7404	B17, C7	74151	A15, K1, K2, K3, K4
N7408	A2, A8, C6, C18, D19, E6, E7, F8, J2, L5, L6, L7, L8, L9, M5, M6, M7, M8, M9	74157	A12, A13, D1, D2, D3, D4, D5
		74193	C1, C2, C3, C4, C5
N7413	D18	7418.0	K5, K6, K7, K8, K9
N7420	B19	74194	F1, F2, F3, F4, F5, H1, H2, H3, H4, H5, H6, H7, H8, H9
N7432	A18, B6, F6, F7, M4, J3		
N7442	M1	N8280	A9, A10, B7, B9, B12, B15, B18, C11, C15, C19, D8, D17, M2
N7473	A14, A16		
N7474	A11, B8	N8273	C8, C9, E9, J1
N7483	E1, E2, E3, E4, E5	N8281	B13, B16
N74[illegible]5	[illegible], B3, L4, B5, J4, J5, J6, J7, J8, J9	N8288	B10, B14
N7416	B11	MC4024P	C14
[illegible]	A4, A5, A17, C10, D6, D7, D9, E8, L2, L3, F9	MC4044P	C13
		7805	D16

NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .03 XXX ± .010 ANGLES ± 1/2°

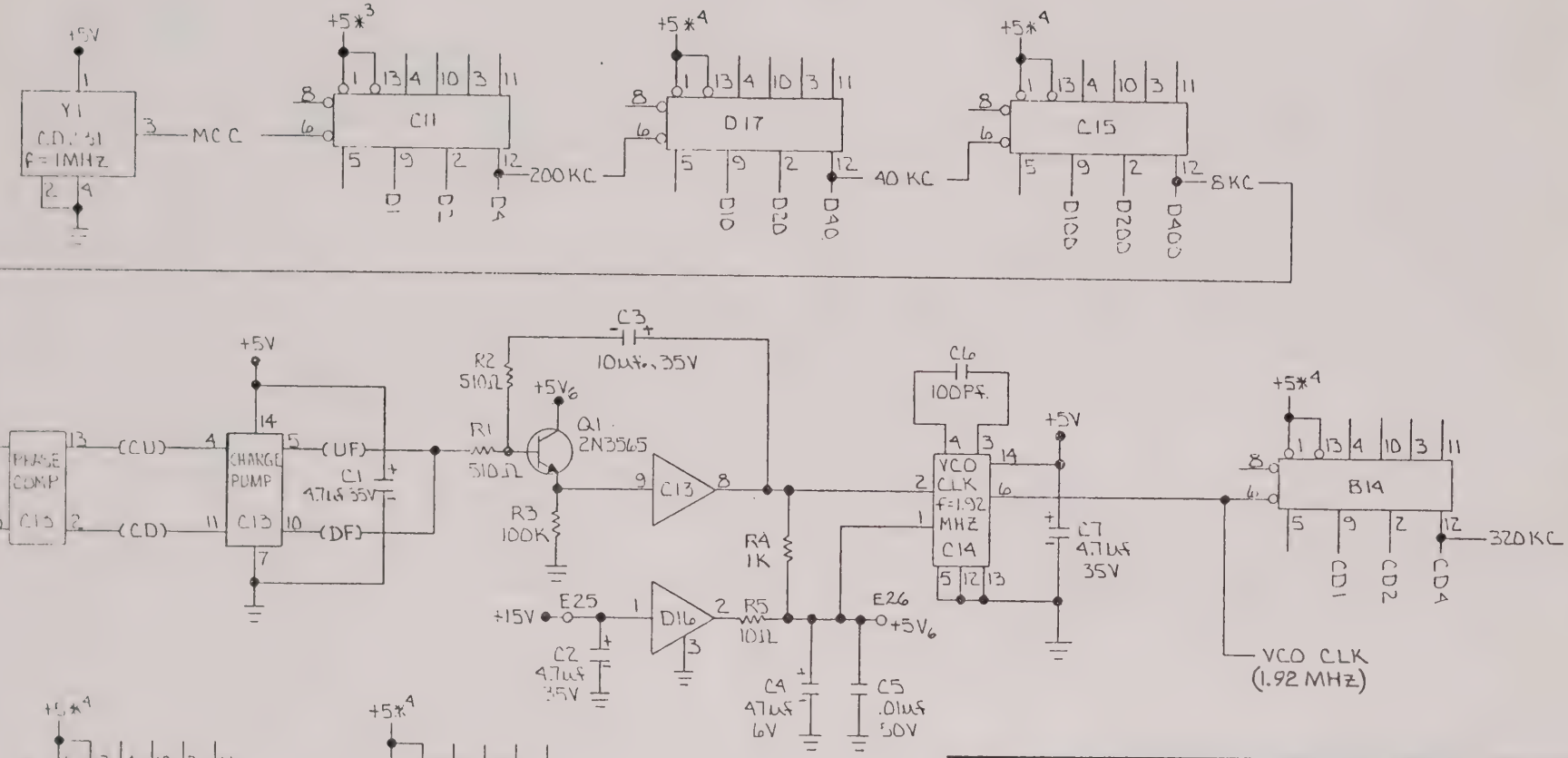
TITLE: DIGITAL READER

DWN: CARY 7/15 | DES: PHL 7/15/75 | CHK: | ENGR: 7/17 7/16/76 | SCALE: NONE | FSC: 31160

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B | 16785 | SIZE | SHT 1 OF 16 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .03, XXX ± .010, ANGLES ± 1/2°

TITLE: DIGITAL READER (1) (1.92 MHZ CLOCK GEN)

DWN	KAIN	8/8/75	DES		8/8/75
CHK			ENGR		
SCALE	NONE		FSC	31160	

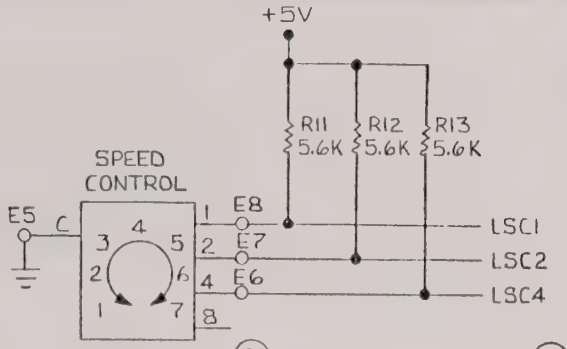
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

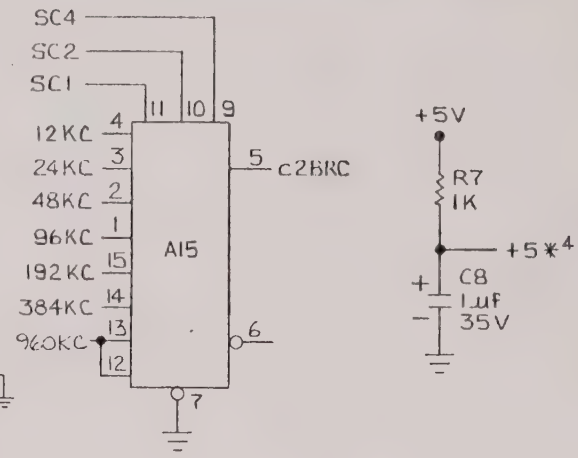
B 16785

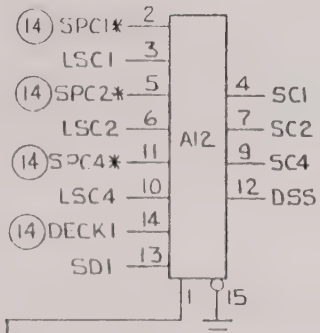
SIZE SHT 2 OF 16 REV

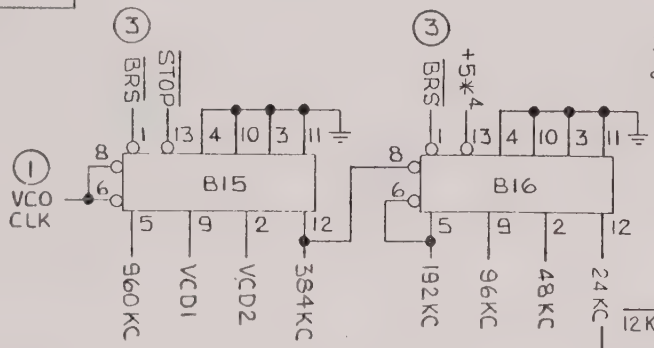
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

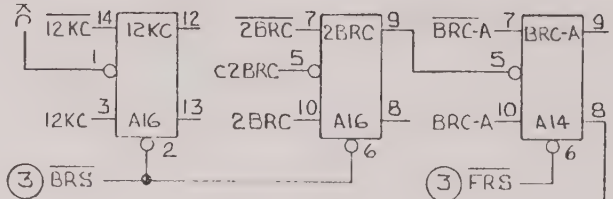
SPEED CONTROL	
POS	TAPE SPEED
1	3 3/4 IPS
2	7 1/2 IPS
3	15 IPS
4	30 IPS
5	60 IPS
6	120 IPS
7	300 IPS

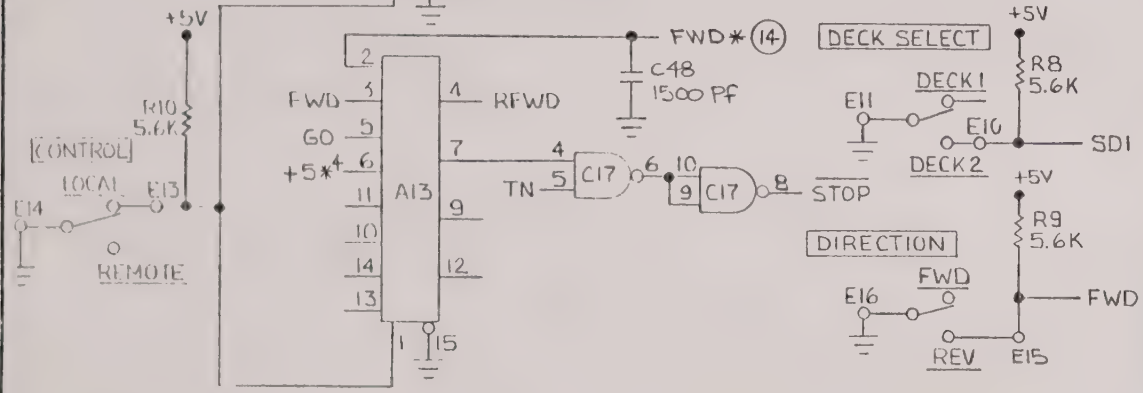












NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

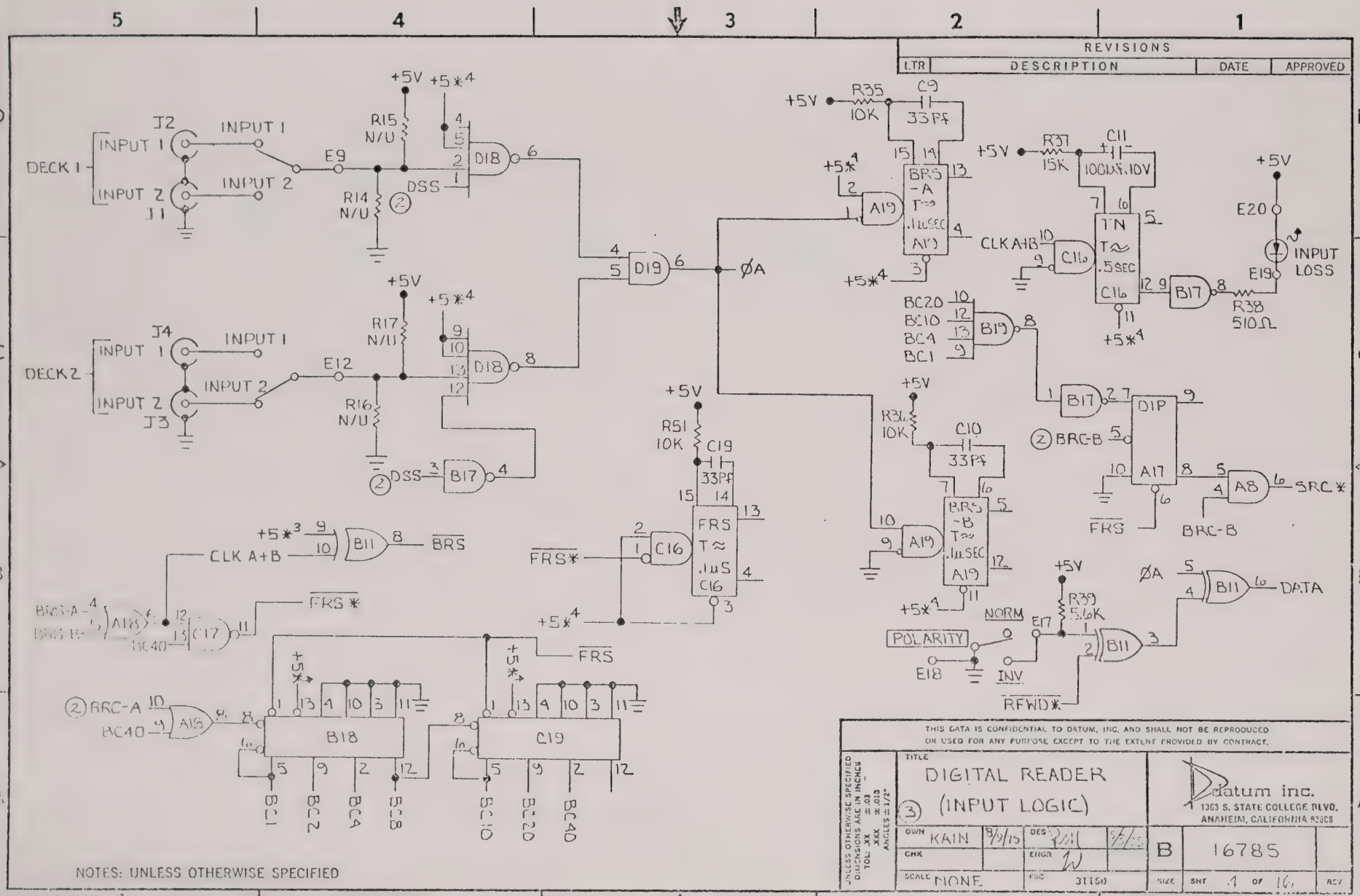
TITLE: DIGITAL READER (CLOCK RATE LOGIC) (2)

DWN	CARY	5/2/75	DES	RML	5/5/75
CHK			ENGR		
SCALE	NONE		FSC	31160	

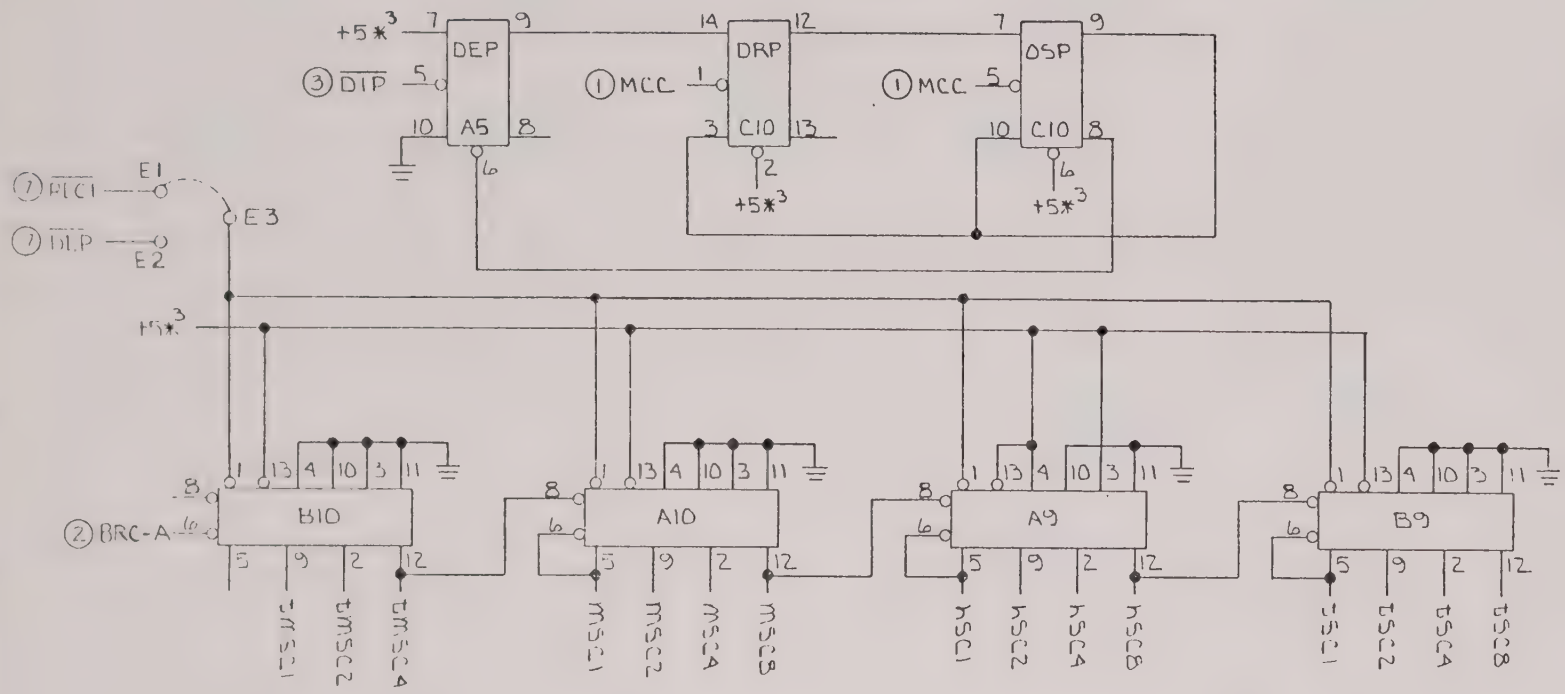
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

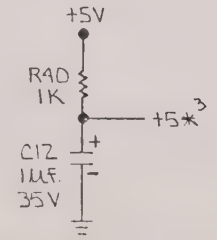
B 16785

SIZE B SHT 3 OF 16 REV


REVISIONS
LTR DESCRIPTION DATE APPROVED
J2 INPUT 1 INPUT 1 DECK 1 INPUT 2 INPUT 2 J1
E9
R15 N/U
R14 N/U
+5V +5*4
DSS
D18
D19
ØA
J4 INPUT 1 INPUT 1 DECK 2 INPUT 2 INPUT 2 J3
E12
R17 N/U
R16 N/U
DSS B17
R35 10K C9 33PF
R37 15K C11 100MF.10V
BRS -A T≈ .1mSEC A19
TN T≈ .5SEC C16
CLK A+B C16 B17
E20 INPUT LOSS E19 R38 510Ω
BC20 BC10 BC4 BC1 B19
R34 10K C10 33PF
BRS -B T≈ .1mSEC A19
D1P A17
BRC-B A8 SRC*
FRS
R51 10K C19 33PF
FRS T≈ .1mS C16
FRS* C16
+5*3 B11 BRS
CLK A+B
BRS-A BRS-B A18 BC40 C17
FRS*
BRC-A BC40 A19
B18 C19
BC1 BC2 BC4 BC8 BC10 BC20 BC40
NORM POLARITY E18 INV E17 R39 5.6K
ØA B11 DATA
RFWD*
NOTES: UNLESS OTHERWISE SPECIFIED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
TITLE
DIGITAL READER
(3) (INPUT LOGIC)
datum inc.
1363 S. STATE COLLEGE BLVD. ANAHEIM, CALIFORNIA 92806
DWN KAIN 8/9/15 DES 8/9/15
CHK ENGR
SCALE NONE FSC 37150
B 16785
SIZE SHT 1 OF 16 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





NOTES: UNLESS OTHERWISE SPECIFIED

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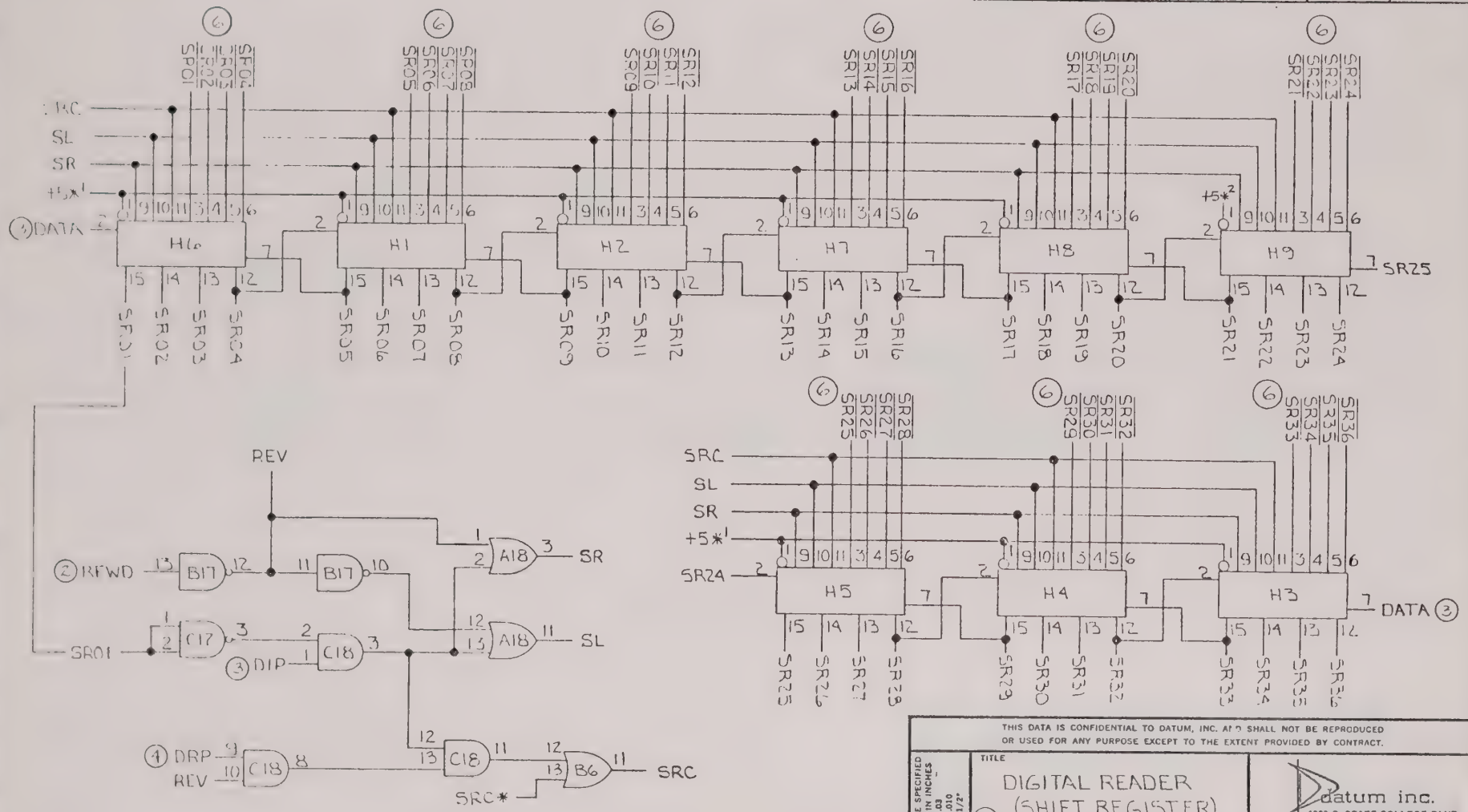
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03, .XXX ± .010, ANGLES ± 1/2°

TITLE: DIGITAL READER (4) (MINOR TIME COUNTER)

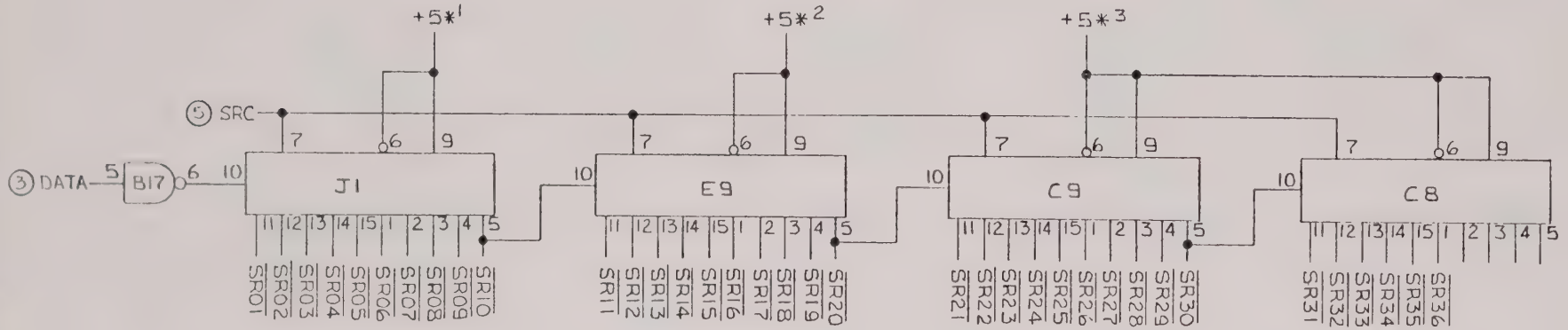
DWN	KAIN	3/13/75	DES		3/13/75
CHK			ENGR		
SCALE	NONE		FSC	31160	

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B | 16785 | SIZE | SHT 5 OF 16 | REV


REVISIONS
LTR DESCRIPTION DATE APPROVED
SRC
SL
SR
+5*1
DATA
H16
H1
H2
H7
H8
H9
SR25
REV
REWD
DIP
DRP
SRC*
SRC
SL
SR
SR24
H5
H4
H3
DATA
NOTES: UNLESS OTHERWISE SPECIFIED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
TITLE
DIGITAL READER (SHIFT REGISTER)
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
DWN KAIN
CHK
ENGR
SCALE
FSC 31160
B 16785
SIZE SHT 6 OF 16 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED

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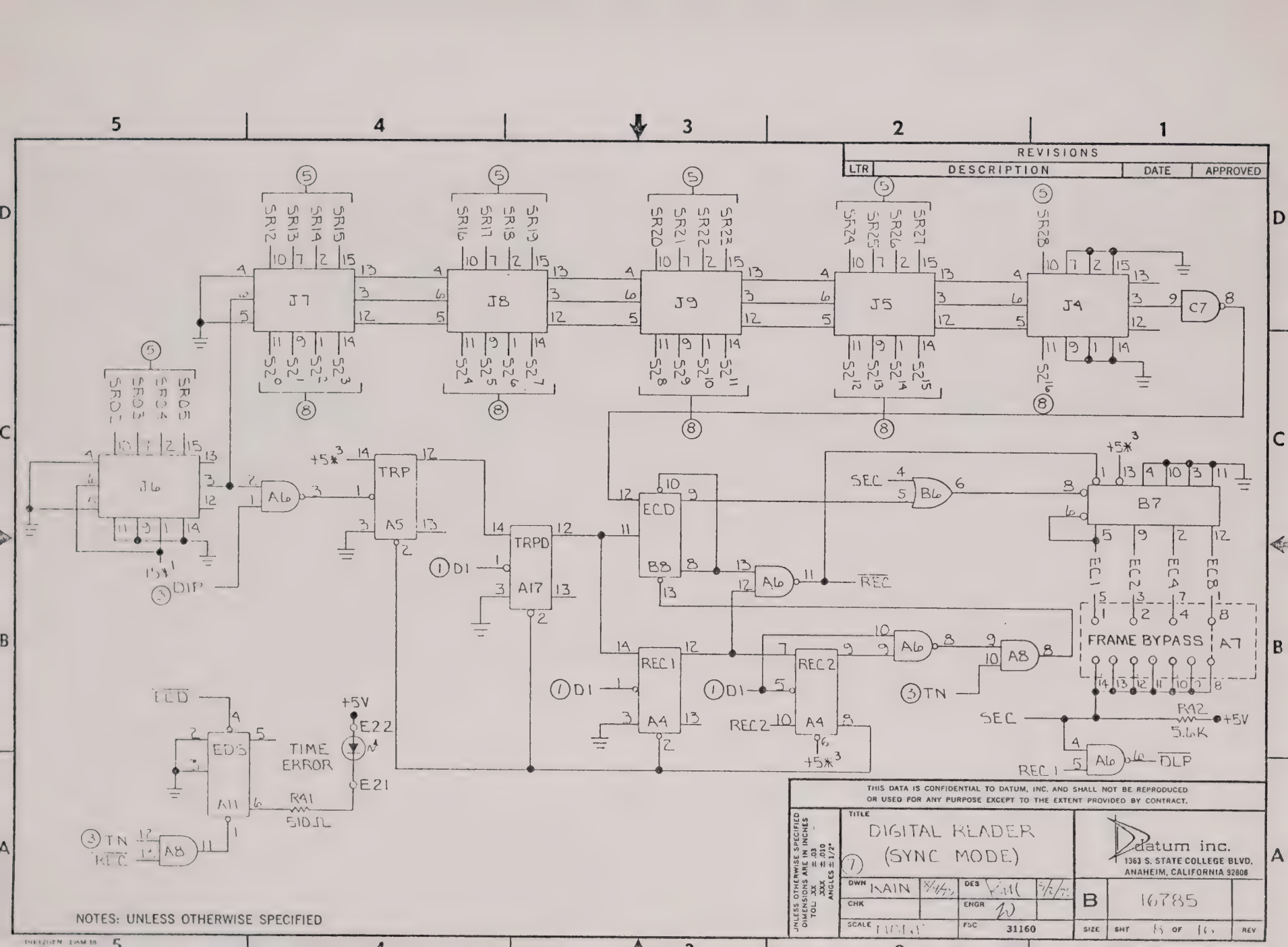
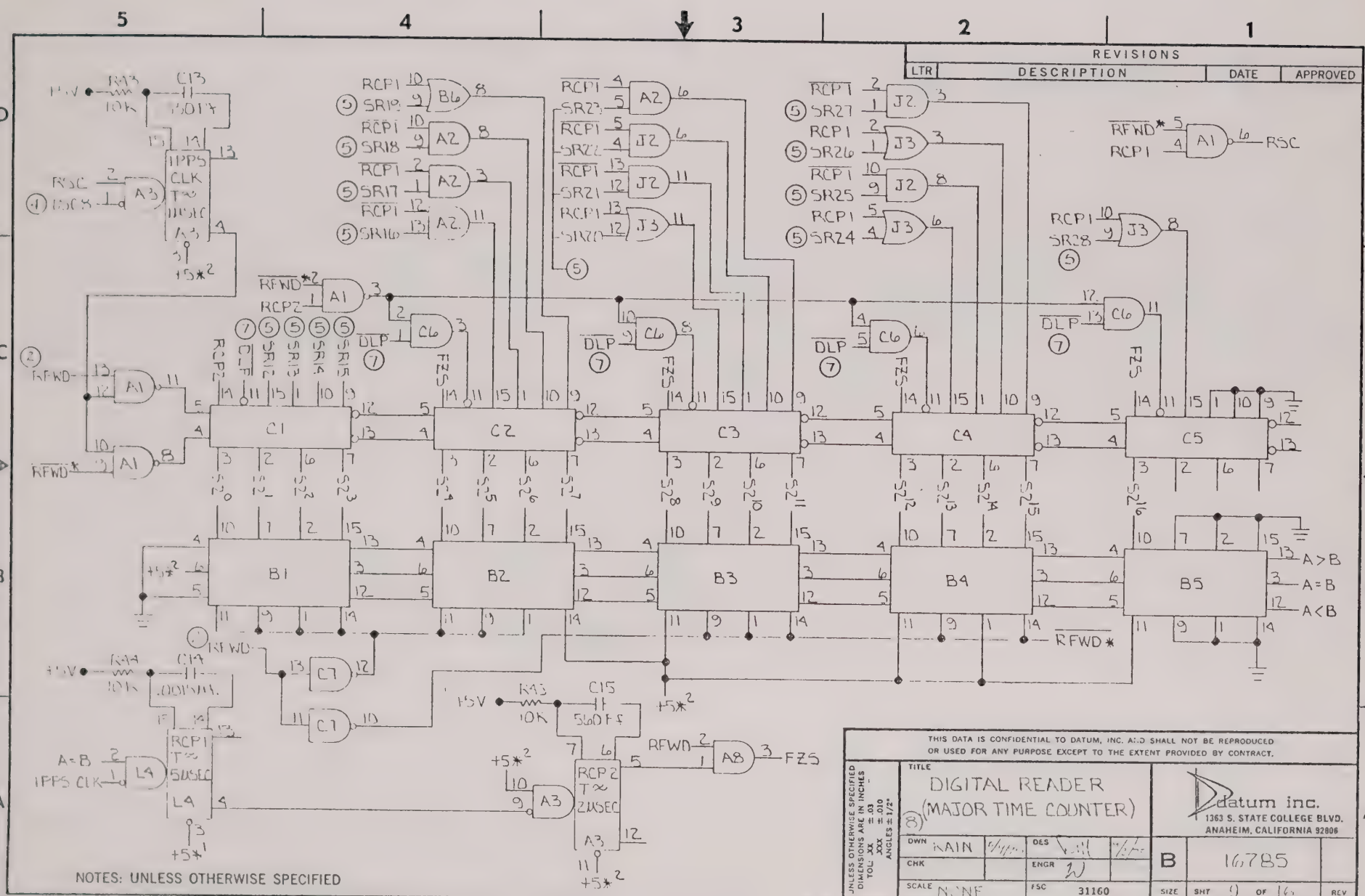
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: DIGITAL READER (SHIFT REGISTER) (6)

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

DWN	CARY	4/4/75	DES	[illegible]	9/4/75	B	16785	
CHK			ENGR	[illegible]				
SCALE	NONE		FSC	31160		SIZE	SHT 1 OF 16	REV


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
J7
J8
J9
J5
J4
J6
C7
B6
B7
A6
A5
TRP
TRPD
A17
ECD
B8
REC1
REC2
A4
A8
A11
EDS
TIME ERROR
R41
510Ω
R42
5.6K
+5V
+5*
SEC
REC
DLP
DIP
D1
TN
FRAME BYPASS
A7
EC1
EC2
EC4
EC8
E22
E21
NOTES: UNLESS OTHERWISE SPECIFIED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
TITLE
DIGITAL READER (SYNC MODE)
datum inc.
1363 S. STATE COLLEGE BLVD. ANAHEIM, CALIFORNIA 92808
DWN KAIN
DES
CHK
ENGR
SCALE
FSC 31160
B
16785
SIZE
SHT 8 OF 16
REV


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
R43
10K
C13
.001MF
1PPS CLK
RSC
A3
+5V*2
RCP1
SR19
SR18
SR17
SR16
B6
A2
RFWD*2
RCP2
A1
C6
DLP
7
FZS
SR27
SR26
SR25
SR24
J2
J3
RFWD*
RSC
SR28
C1
C2
C3
C4
C5
SR0
SR1
SR2
SR3
SR4
SR5
SR20
SR21
SR22
SR23
SR12
SR13
SR14
SR15
SR29
SR30
SR31
SR32
SR33
SR34
SR35
SR36
B1
B2
B3
B4
B5
A>B
A=B
A<B
RFWD*
C7
R44
C14
.001MF.
A=B
1PPS CLK
L4
5USEC
C15
560PF
RCP2
2USEC
A8
FZS
NOTES: UNLESS OTHERWISE SPECIFIED
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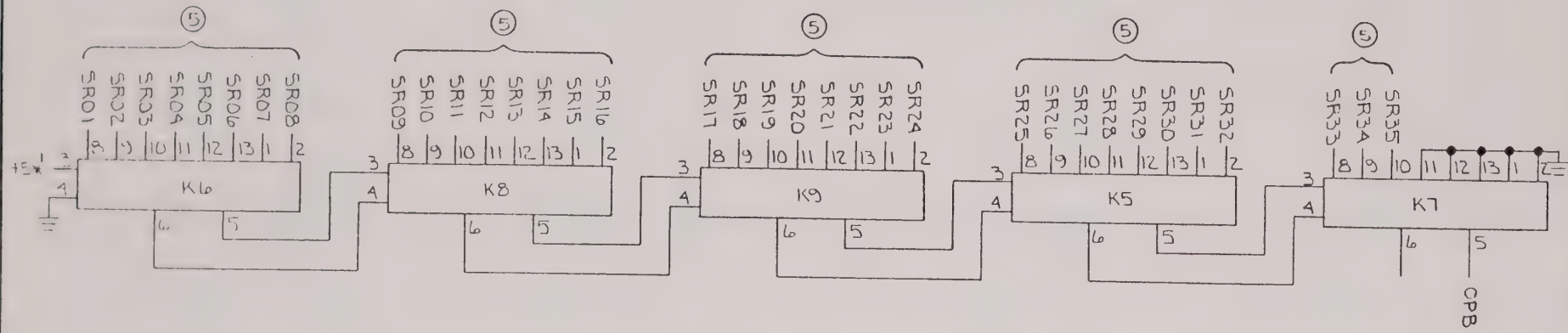
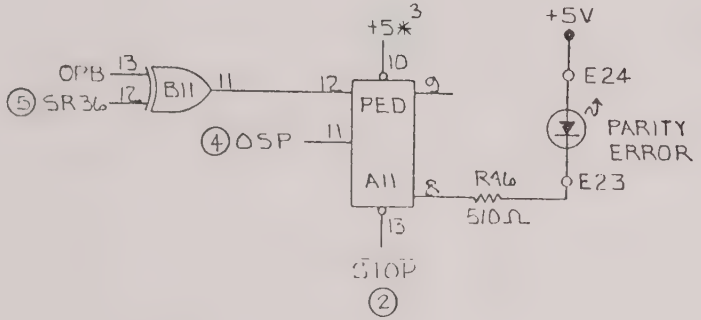
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ±.03 XXX ±.010 ANGLES ±1/2°
TITLE
DIGITAL READER
(8) (MAJOR TIME COUNTER)
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
DWN KAIN
DES
CHK
ENGR
SCALE NONE
FSC 31160
B
16785
SIZE
SHT 9 OF 16
REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





NOTES: UNLESS OTHERWISE SPECIFIED

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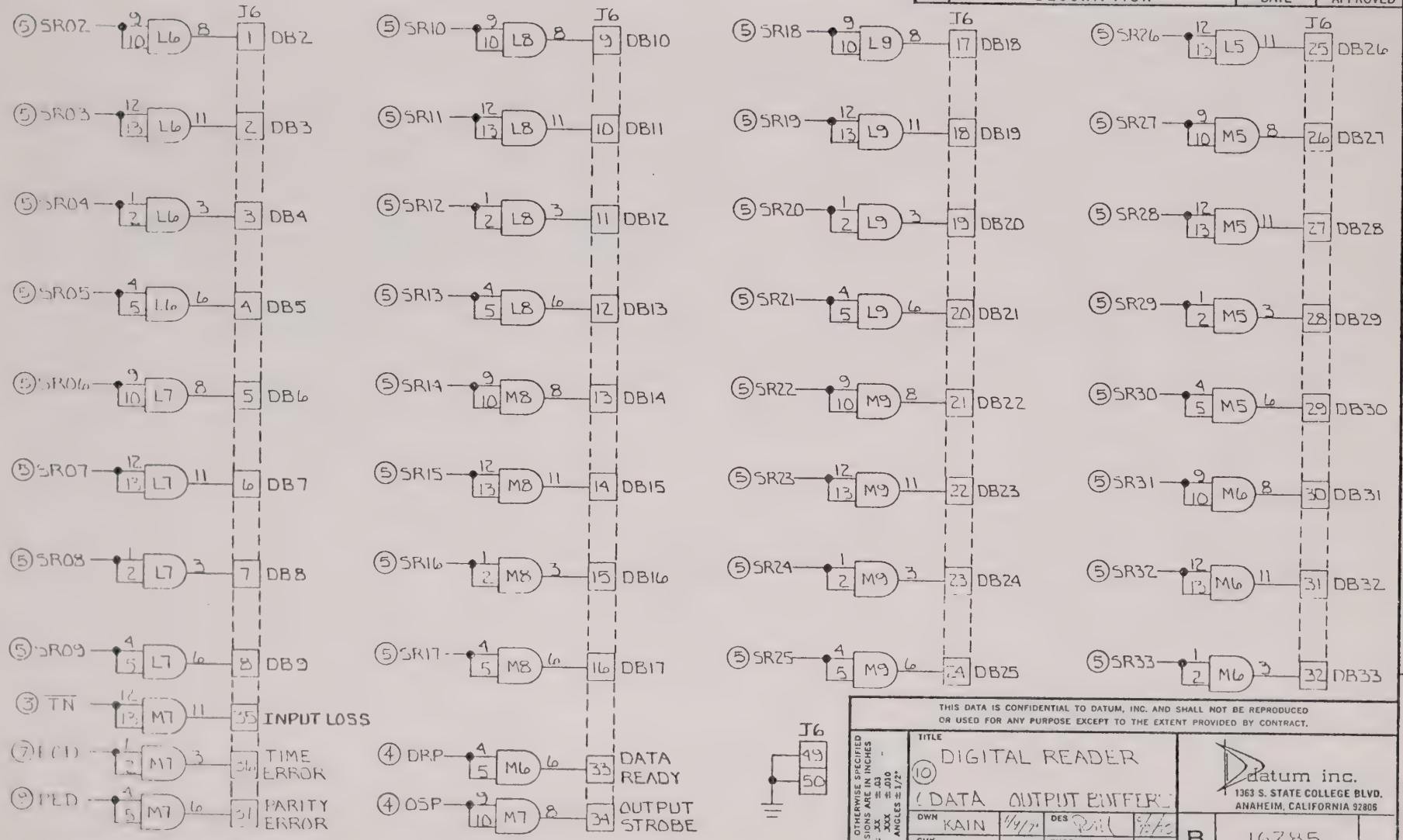
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: DIGITAL READER (PARITY ERROR DET)

DWN KAIN	5/9/75	DES		9/2/75
CHK		ENGR		
SCALE NONE		FSC 31160		

Datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92805

SIZE	DRAWING NO.	REV
B	16785	
SHT 10 OF 16		



NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

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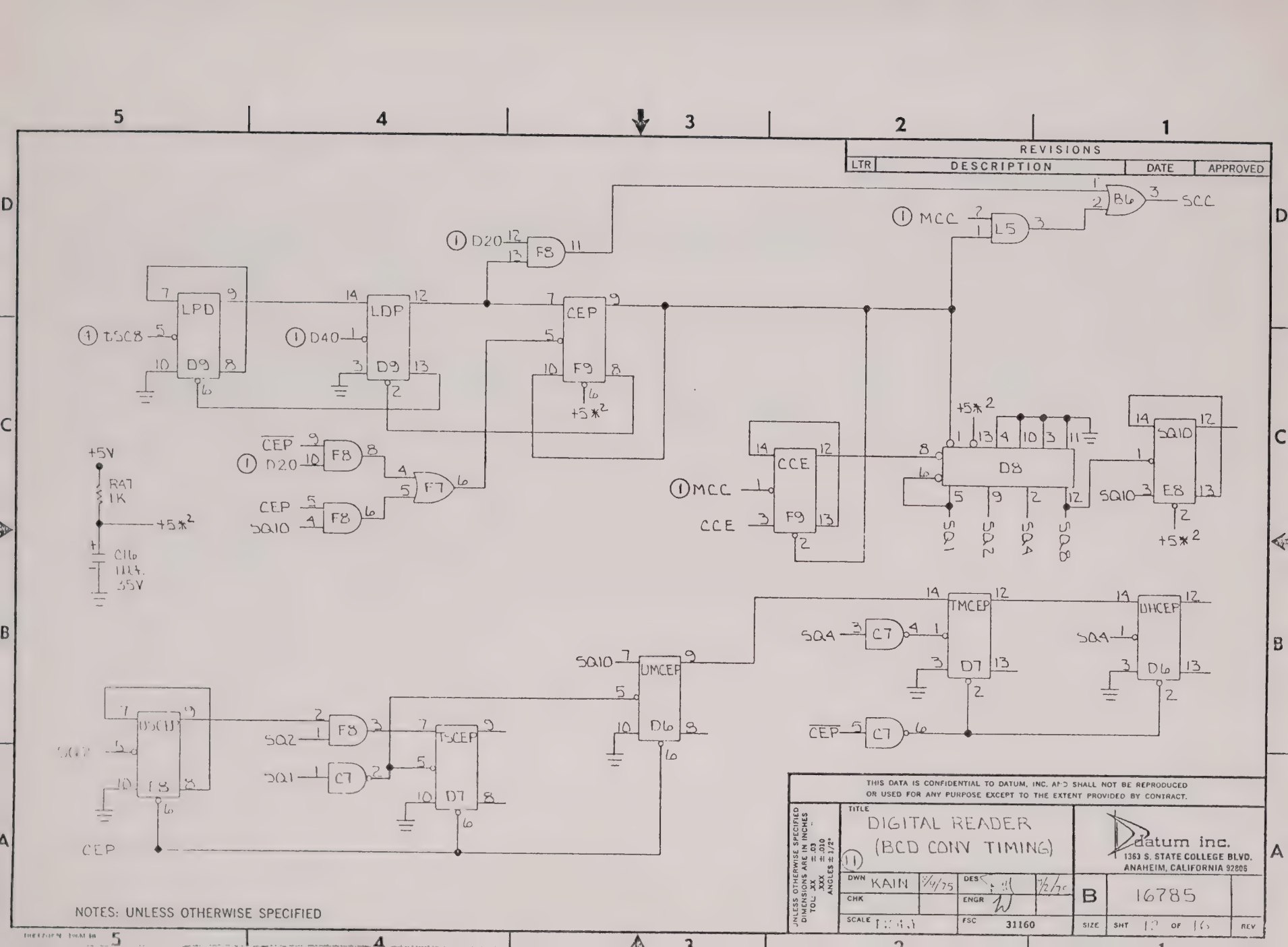
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ±.03, XXX ±.010, ANGLES ±1/2°

TITLE: (10) DIGITAL READER (DATA OUTPUT BUFFER)

DWN KAIN	11/9/77	DES	
CHK		ENGR	
SCALE NONE		FSC 31160	

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B | 16785 | SIZE | SHT 11 OF 16 | REV


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
SCC
MCC
B6
L5
D20
F8
LPD
LDP
CEP
D9
F9
TSC8
D40
+5V
R47
1K
+5*2
C116
1UF.
35V
CEP
D20
F8
F7
SQ10
CCE
MCC
F9
D8
SQ1
SQ2
SQ4
SQ8
E8
TMCEP
UMCEP
TSCEP
C7
D7
D6
SQ4
SQ2
SQ1
SQ10
CEP
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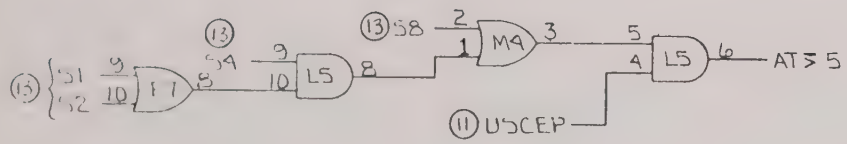
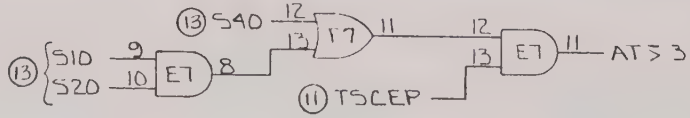
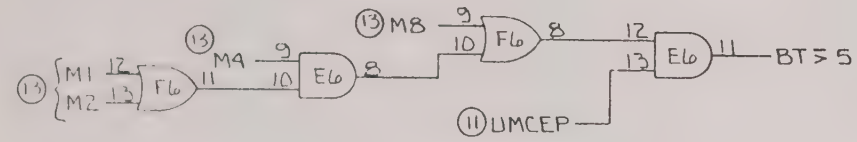
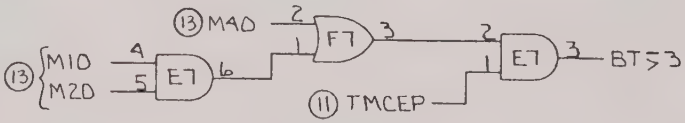
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
TITLE
DIGITAL READER
(BCD CONV TIMING)
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
DWN KAIN 7/1/75
CHK
DES
ENGR
SCALE
FSC 31160
B
16785
SIZE
SHT 12 OF 16
REV
NOTES: UNLESS OTHERWISE SPECIFIED

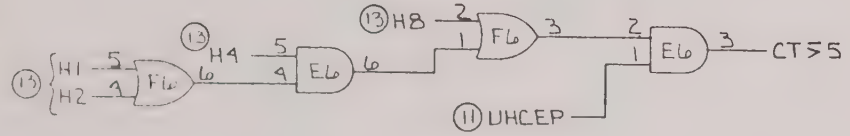
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED











NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE
DIGITAL READER
(12) (CONVERT ENABLE LOGIC)

DWN	KAIN	6/4/75	DES		8/26/75
CHK			ENGR		
SCALE	NONE		FSC	31160	

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

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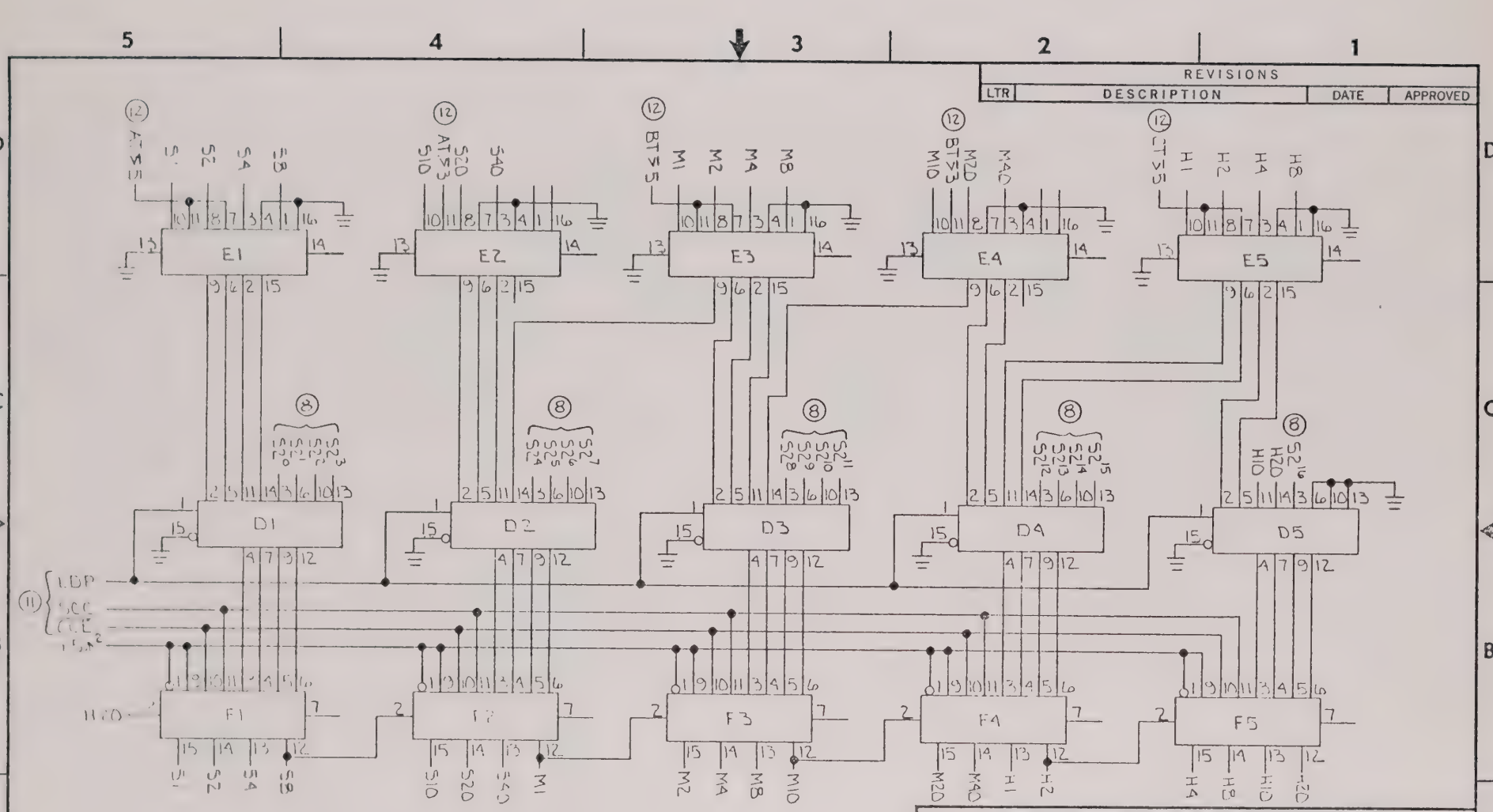
SIZE SHT 13 OF 13 REV



NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

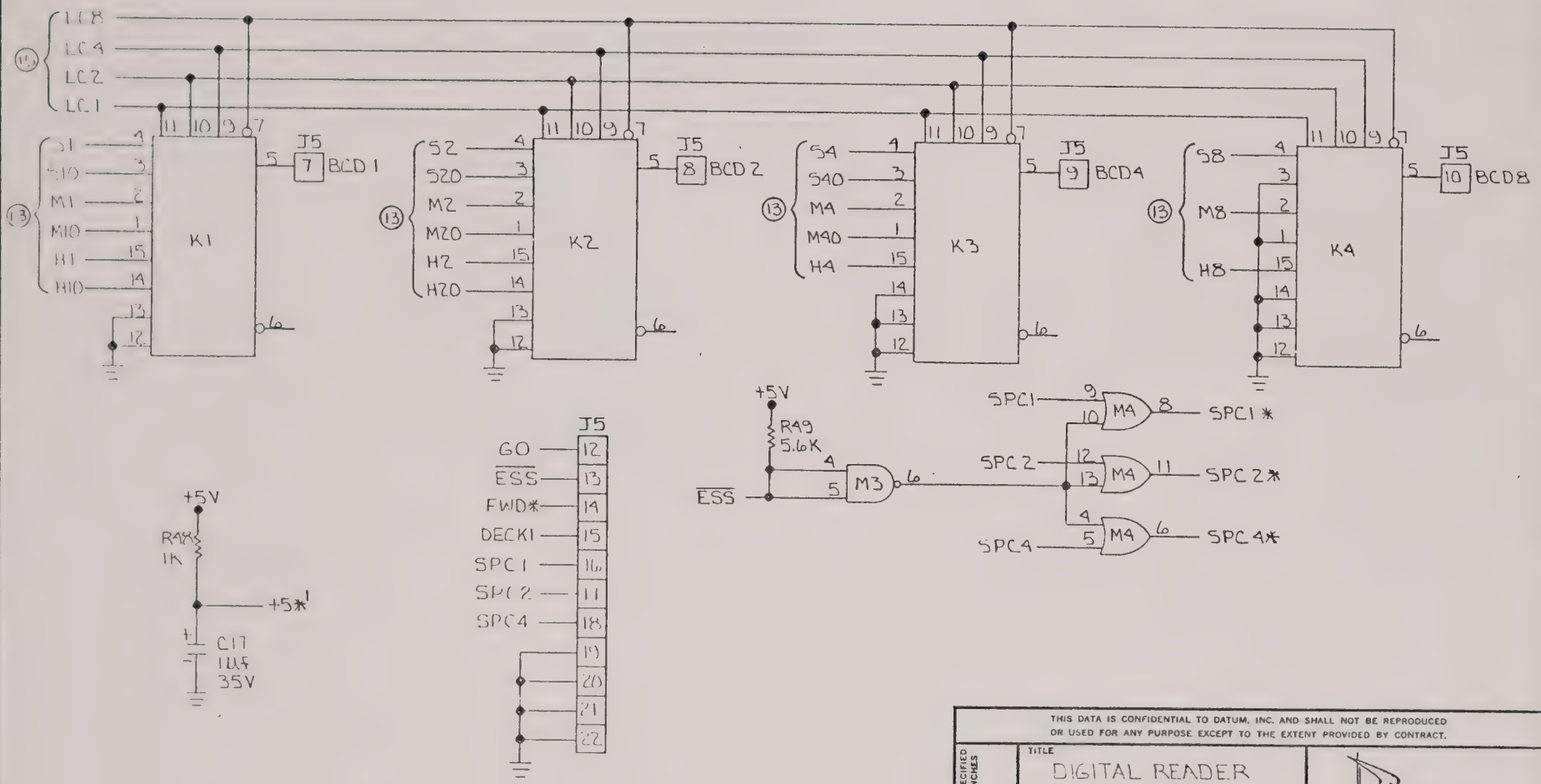
TITLE
DIGITAL READER
(BIN TO BCD S-M-H CONV)

DWN KAIN 7/11/73 DES 7/11
CHK ENGR
SCALE NONE FSC 31160

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B 16785
SIZE SHT 14 OF 16 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL- .XX ±.03 .XXX ±.010 ANGLES ± 1/2°

TITLE
DIGITAL READER
(I/O CONTROL)
(14)

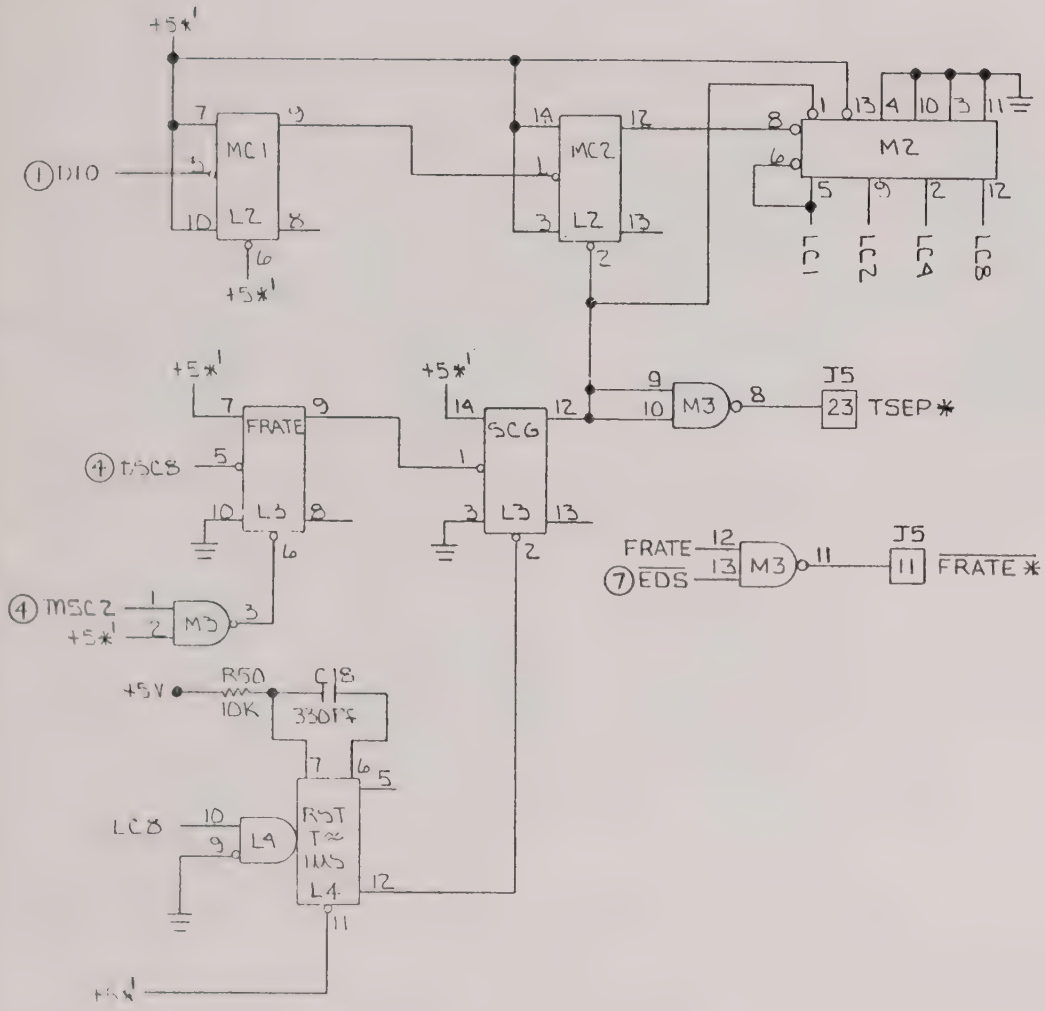
DWN	KAIN 8/1/75	DES		
CHK		ENGR		
SCALE	NONE	FSC	31160	

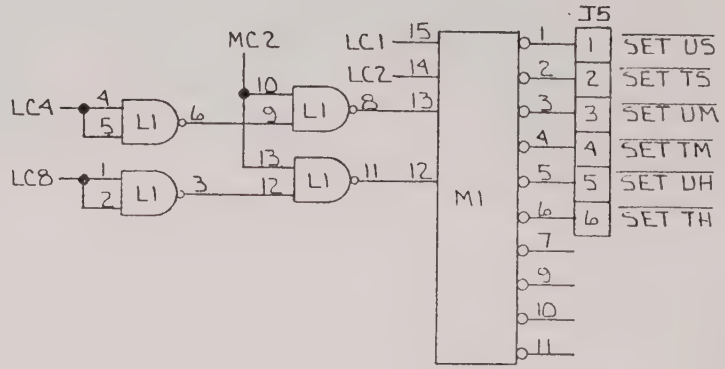
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B 16785

SIZE SHT 15 OF 16 REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





NOTES: UNLESS OTHERWISE SPECIFIED

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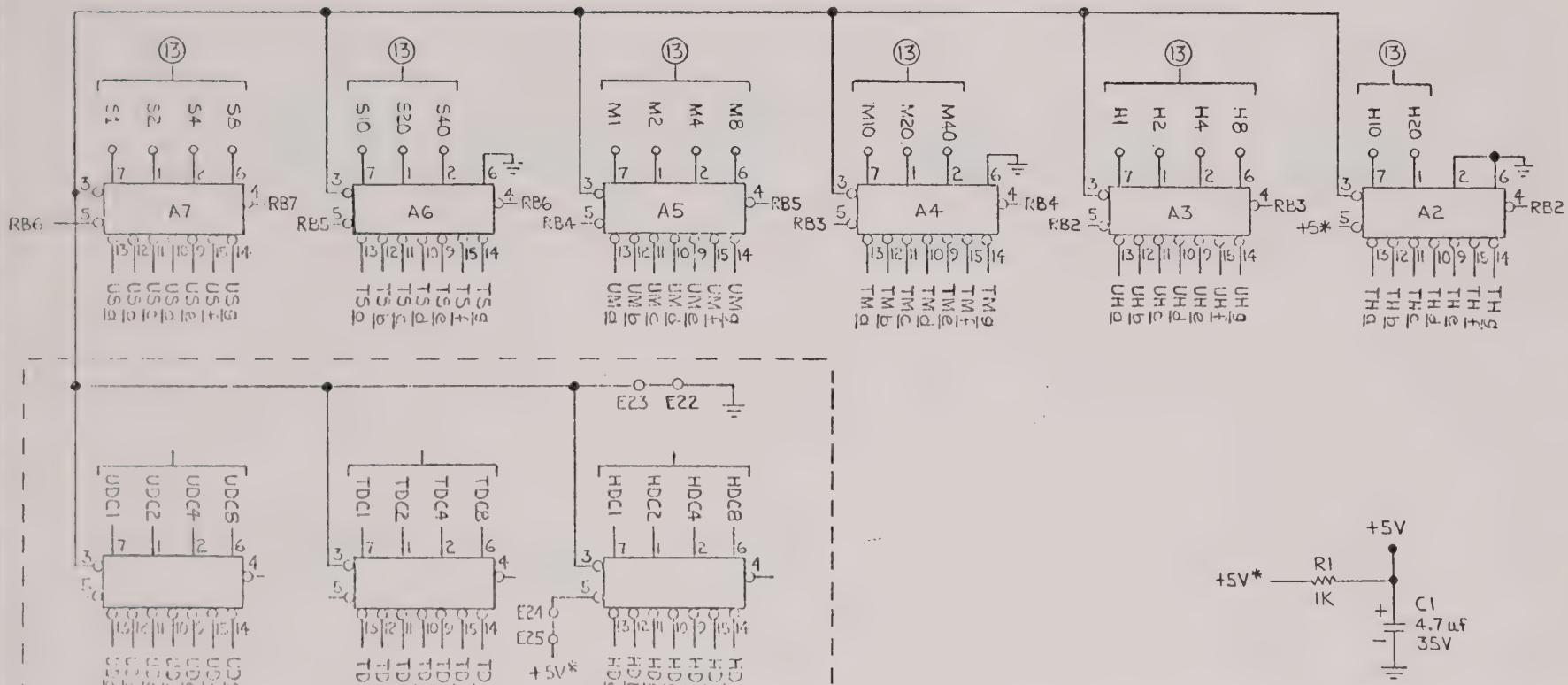
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.03 .XXX ±.010 ANGLES ±1/2°

TITLE: DIGITAL READER (15) (OUTPUT MUX SCAN)

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

DWN KAIN	8/4/75	DES			
CHK		ENGR			
SCALE NONE		FSC 31160	SIZE B	16785	REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



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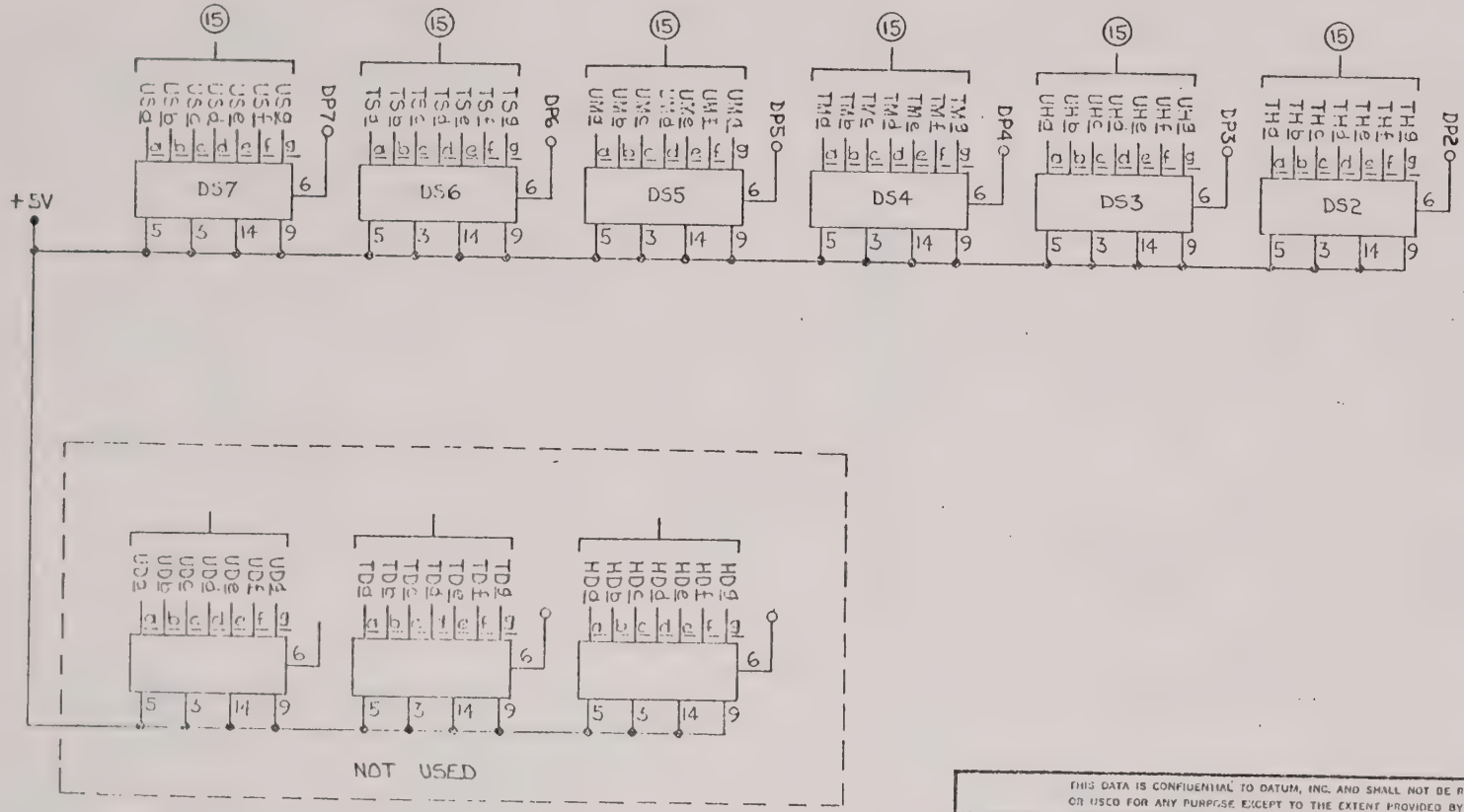
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: LED DISPLAY (DRIVERS) (16)

datum inc.
1363 S. STATE COLLEGE BLVD
ANAHEIM CALIFORNIA 92805

DRN	J.C.	8/Feb/15	DES			
CHK			ENGR	W.	11/9/76	B 16832
SCALE	NONE		FSC	31260	SHT	1 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



- 3 LEDS ARE FAIRCHILD FND-507
- 2 LEDS ARE MONSANTO MAN6A
1. LED'S ARE DIP 5082-7750

NOTES: UNLESS OTHERWISE SPECIFIED

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TITLE: LED DISPLAY (17)

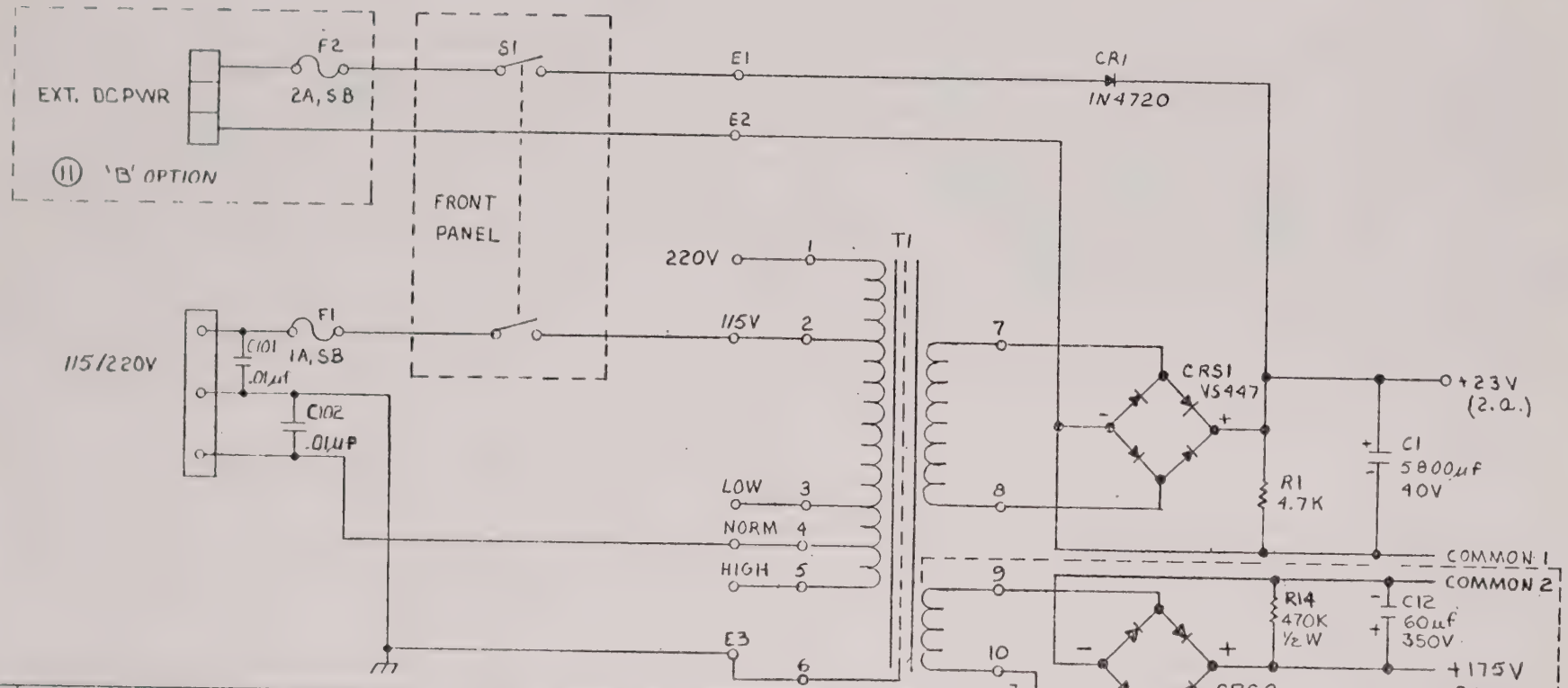
DWN	J.C.	8/28/75	DES
CHK			ENGR
SCALE	NONE		FSC 01100

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B 16832

SIZE | SHT 2 OF 2 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	C4 WAS 948901 SELECTED 47μf	6-26 73	RM



A	INCLUDES ASSY 16742		
-10	+5V, ±8V	C12, CRS2, R14	956082
-9	-1, -3, -5, OR -7 USED WITH 16742		
-8	+5V, ±12V, -15, +175	C12	956088
DASH NO.		COMP. NOT USED	XFORMER USED
NOTES: UNLESS OTHERWISE SPECIFIED			

-7	+5V ± 15V	C12, CRS2, R14	956116
-6	+5V ± 15V +175V	C12	956088
-5	+5V, +12V, -15V	SEE NOTE 5.	956082
-4	+5V ±15V, +175V		956088
-3	+5V, ±15V	C12, CRS2, R14	956082
-2	+5V, +175V	A2, A3, C8, C9, C10, C11, CR7, CR8	956088
-1	+5 ONLY	A2, A3, C8, C9, C10, C11, C12, CR7, CRS2, R14, CR8	956082
DASH NO.		COMP 3 NOT USED	XFORMER USED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: POWER SUPPLY

(49)

DWN	EK	3/23/73	
CHK			
SCALE	NONE	DES	3/30
ENGR			4/2/73
PSC	31160		

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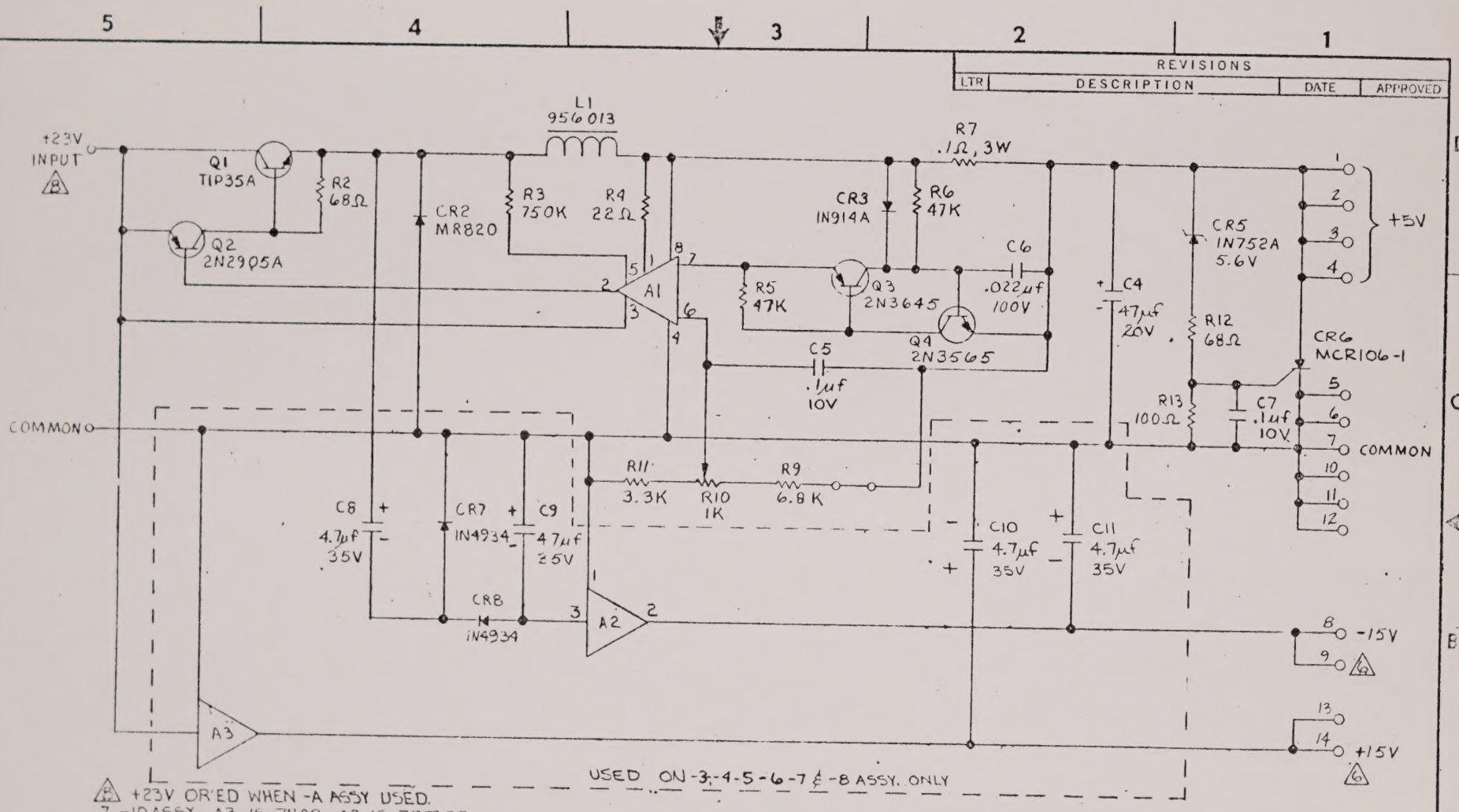
B | 16280 | A

SIZE | SHT 1 OF 2



NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE 1/4 W 5%
2. A1 IS LM305
3. A2 IS LM320-15H
4. A3 IS UGA7815393 OR MC7815CP
5. -5 ASSY. A3 IS UGA7812393 OR MC7812CP
6. -5 & -8 ASSY. OUTPUT IS +12V, -10 ASSY OUTPUT IS ±8V
7. -10 ASSY. A3 IS 7808, A2 IS 79M08.
8. +23V OR'ED WHEN -A ASSY USED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX = .03 .XXX = .010 ANGLES = 1/2°

TITLE: REGULATOR (49)

DWN EK 3/22/73 | DES John 3/30

CHK | ENGR MHP 6/73

SCALE NONE | FSC 31160

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B | 16280 | A

SIZE | SHT 2 OF 2

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